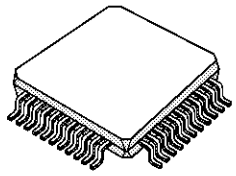
SGS-THOMSON MICROELECTRONICS

ST75C50

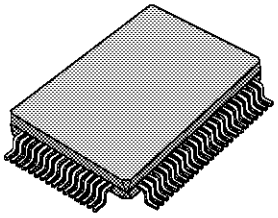
V.32bis/V.17 HIGH SPEED MODEM DATAPUMP

ADVANCE DATA

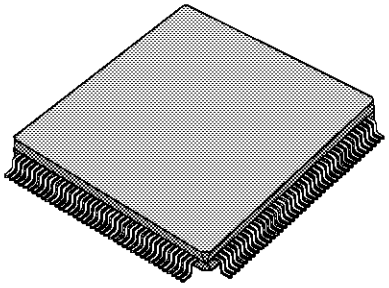
- 2 AND 4 -WIRE FULL DUPLEX OPERATION
- V.32BIS, V.17, V.33, V.32, V.29, V.27ter, V.22BIS, V.22, V.21, V.23, BELL212A, 103
- GROUP 3 FAX AT 14400, 12000, 9600, 7200, 4800, 2400BPS
- PARALLEL/SERIAL SYNCHRONOUS DATA HANDLING
- DIGITAL FAR AND NEAR END ECHO CANCELLATION SUPPORTING A DELAY OF 2 SATELLITE HOPS (1.6 seconds) AND PHASE ROLL UP TO 10Hz
- AUTODIAL AND AUTOANSWER
- COMPLETE HANDSHAKE MANAGEMENT
- WIDE DYNAMIC RANGE (> 48dB)
- COMPROMISE TRANSIT EQUALIZER
- AUTOMATIC ADAPTIVE EQUALIZER
- VOICE MODE (A LAW)
- ENHANCED PROGRAMMABLE TONE DETECTOR (INCLUDING DTMF)
- AUTO MODE
- MULTILEVEL OPERATING SOFTWARE
- CCITT V.54 SIGNALLING
- ANCILLARY CONVERTERS FOR EYE PATTERN MONITORING
- VERSATILE INTERFACES
  - PARALLEL 64x8 DUAL PORT RAM
  - SYNCHRONOUS SERIAL I/O
  - AUXILLIARY PARALLEL I/O
- CALLER ID DEMODULATION
- PROGRAMMABLE HOST MCU INTERRUPT RATE
- SIMPLE CUSTOMISATION / EXTENSION OF FUNCTIONALITY
- LOW PROFILE TQFP PACKAGE OPTION
- MONOPACKAGE DATAPUMP OPTION



TQFP44
(Plastic Quad Flat Pack)



PQFP80
(Plastic Quad Flat Pack)



PQFP160
(Plastic Quad Flat Pack)

ORDERING INFORMATION

Sales Type	Function	Package
ST75C50	Monopackage Datapump	PQFP 160
ST7543 CQFP	Mafe	TQFP 44
ST7543 CNF	Mafe	PLCC 44
ST75C500 CQFP	Romed DSP	TQFP 80
ST75C500 PQFP	Romed DSP	PQFP 80
ST75C500 EQFP	Romed DSP with access to external additional memory	PQFP 160
ST18933 PQFP	Customisable DSP	PQFP 160
ST75C50 DEMOI	Modem	BOARD
STI8933 EMU-PC	PC Software Developement Tool	PC BOARD

SUMMARY

APPENDIX

I - GENERAL DESCRIPTION

This highly integrated modem consists of 2 chips, the first being a dedicated DSP (ST75C500), the second being the ST7543 MAFE. Emphasis has been put on performance and size/power consumption for portable applications.The chipset is supplied in either single package or two package form.

This product gives a high performance modem conformant to CCITT recommendations V.32bis, V.17, V.33, V.32, V.29, V.27ter, V.22bis, V.22, V.21 and V.23. Also Bell 212A and 103.

As a data modem the ST75C50 can operate at 14400, 12000, 9600, 7200, 4800, 2400, 1200, 300 or 75 bits per second as standard. As a fax, the ST75C50 fully supports group 3 send and receive speeds of 14400, 12000, 9600, 7200, 4800 and 2400 bits per second.

Programmable features allow the product to be tailored to a wide range of high speed modem requirements.In addition, to add to the flexibility of this product, the customer can develop, on a similar hardware platform to the standard product, proprietry code for ROMing into the memory of the DSP. If required, ability to access external memory of upto 64K x 32 is given such that customer specific modes of operation can be added and easily updated.Code development is made simple via a slot in PC development card and is fully supported by SGS-THOMSON (STI8933 PC-EMU).

The voice mode allows for implementation of enhanced telephony functions such as answering machines. Incoming samples from the line are PCM-A-law coded and are written into the dual port RAM. The outgoing samples are decompressed using the same A-law and are output to the telephone line.

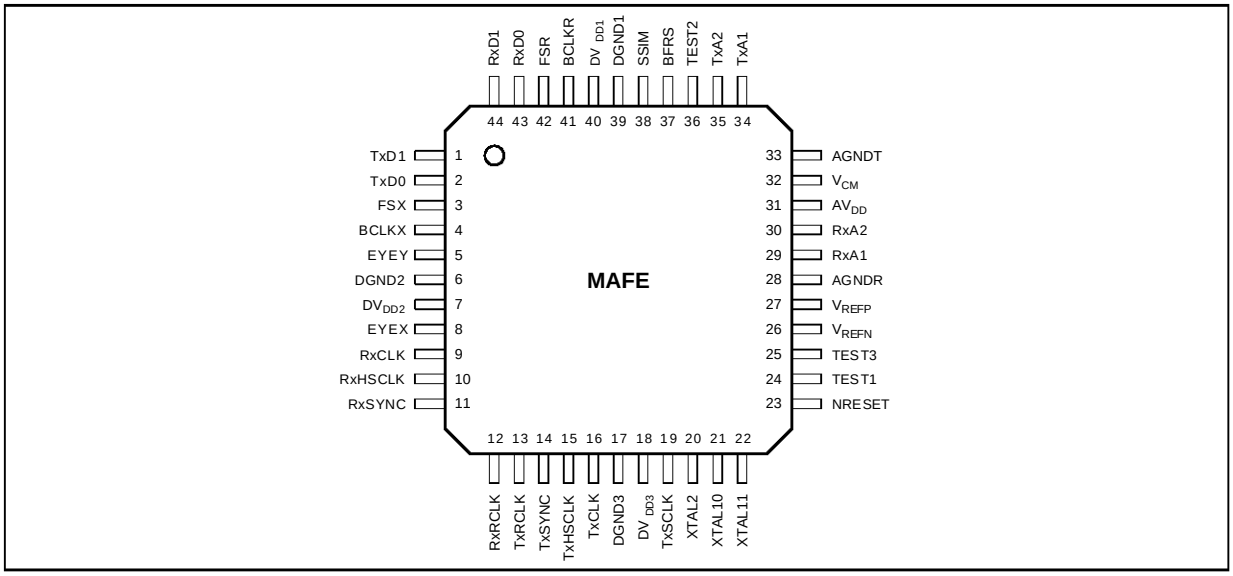
The modem standard products are packaged in either a 160 pin plastic quad flatpack or two flatpacks for low profile applications (one 44 pin and the other 80 pin).

For customer specific code requiring access to external memory, a 160 pin flatpack containing the DSP and a 44 pin flatpack containing the MAFE are also available (type numbers ST18933 and ST7543 respectively).

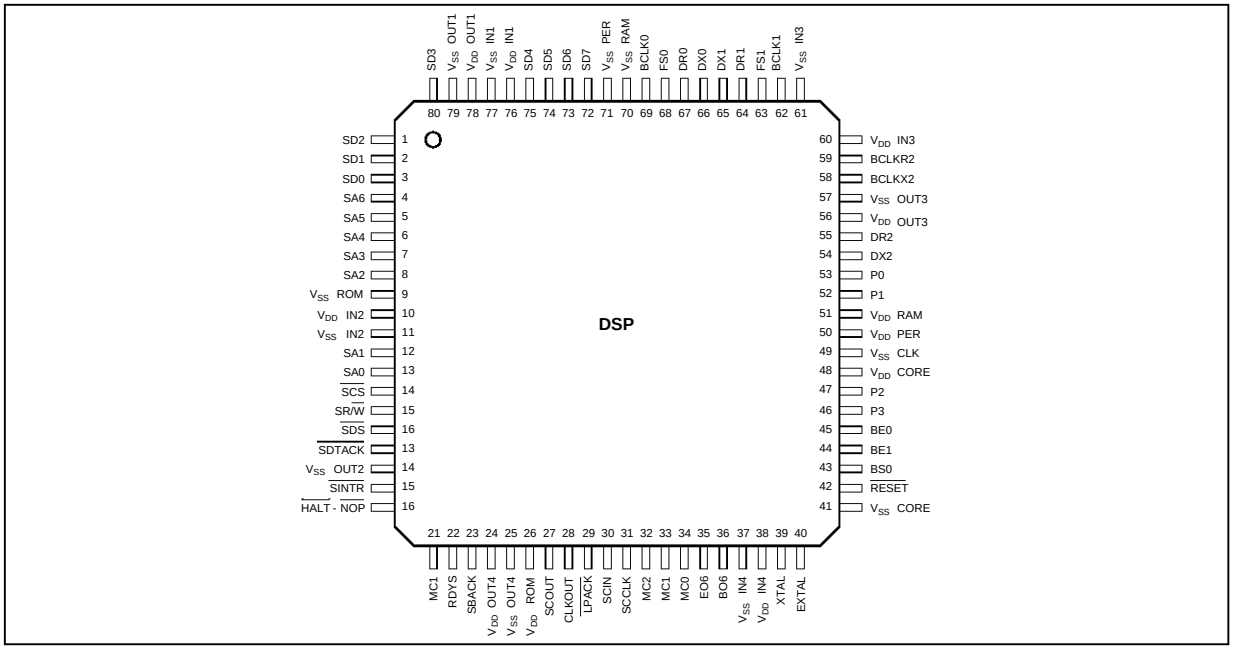
Further information on the DSP (STI8933) and MAFE (ST7543) can be found in the relevant datasheets

II - PIN CONNECTIONS

II.1 - ST7543CQFP Top View (TQFP44)

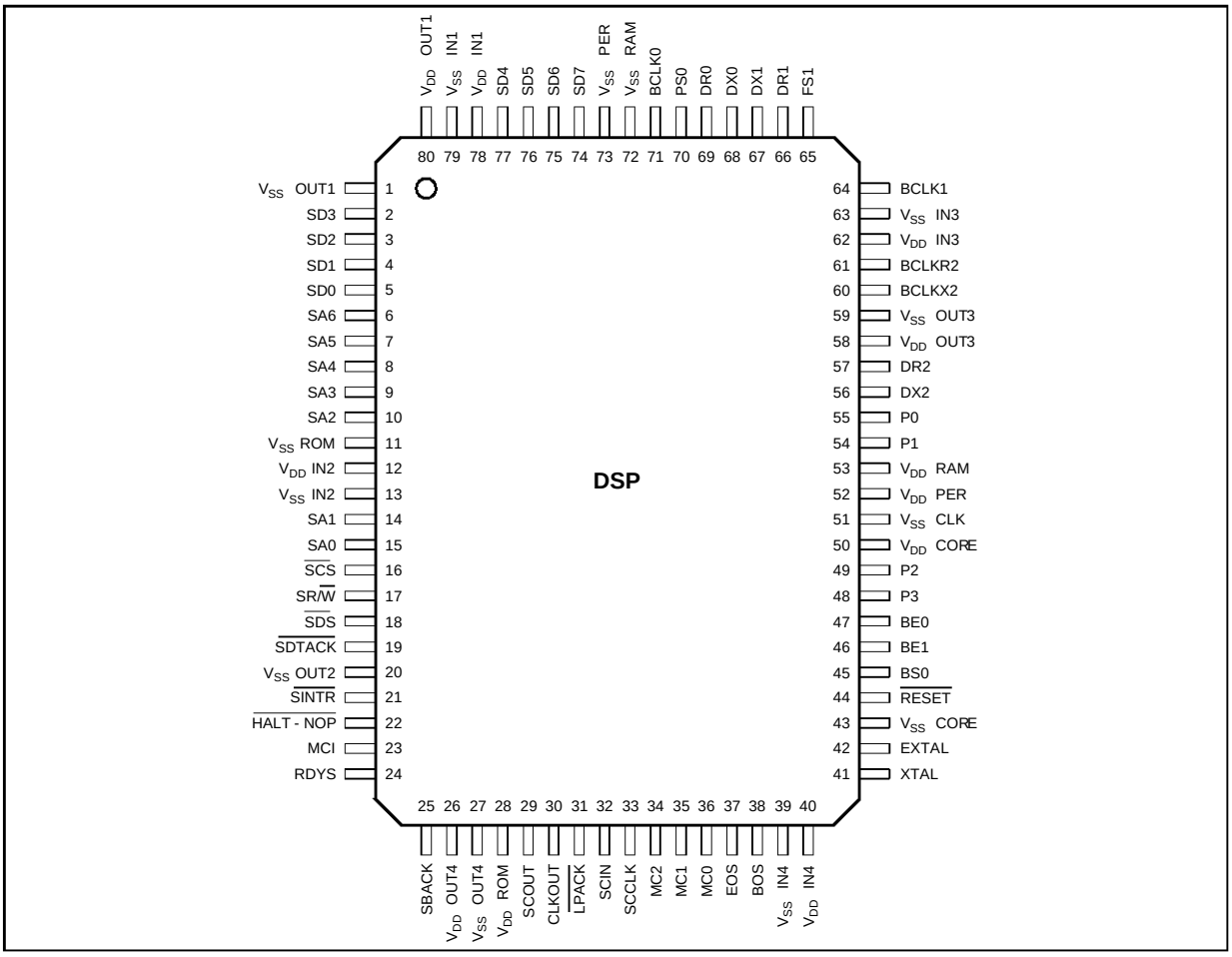


II.2 - ST75C500CQFP Top View (TQFP80)



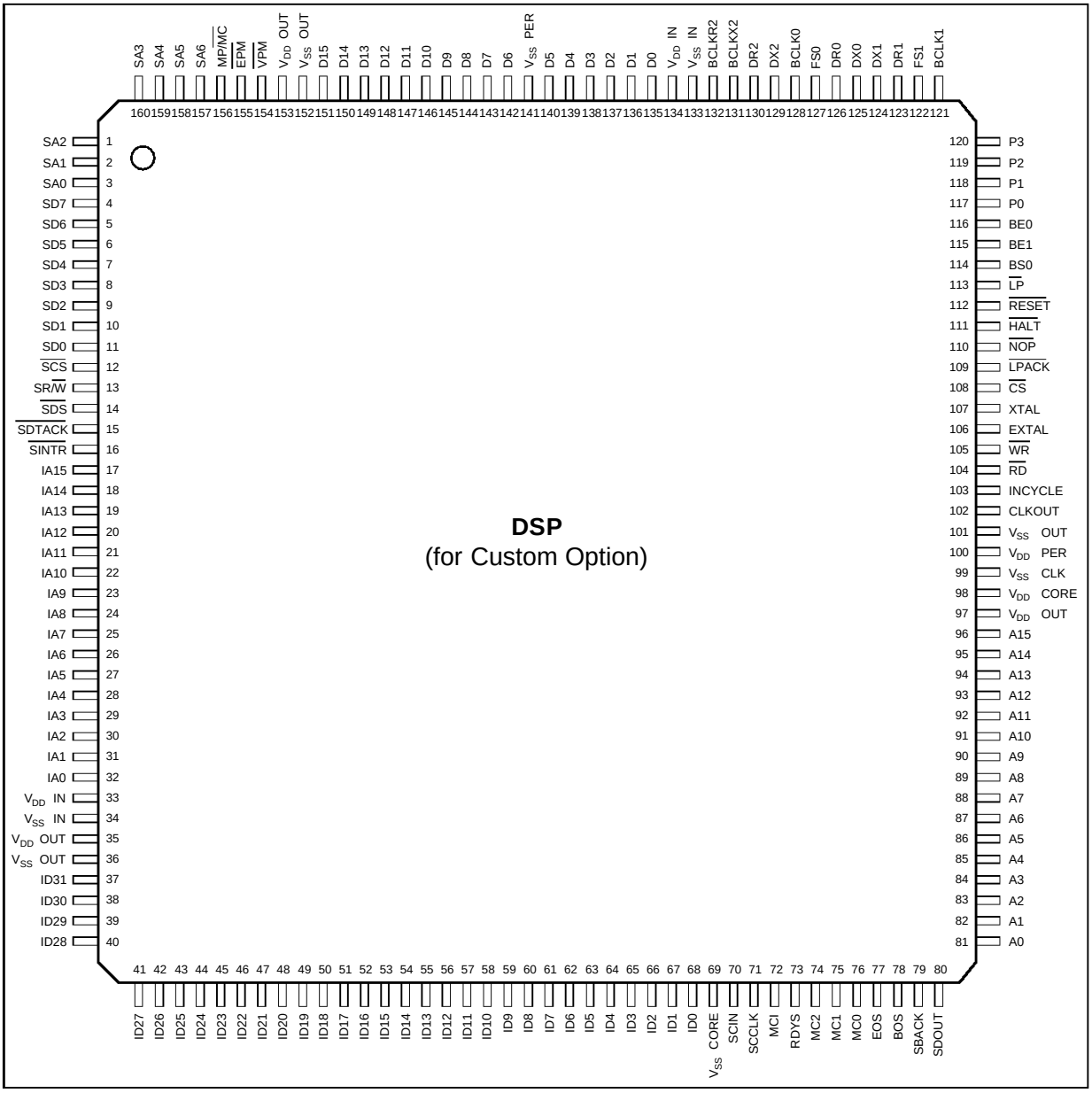
75C50-02.EPS

II.3 - ST75C500PQFP Top View (PQFP80)

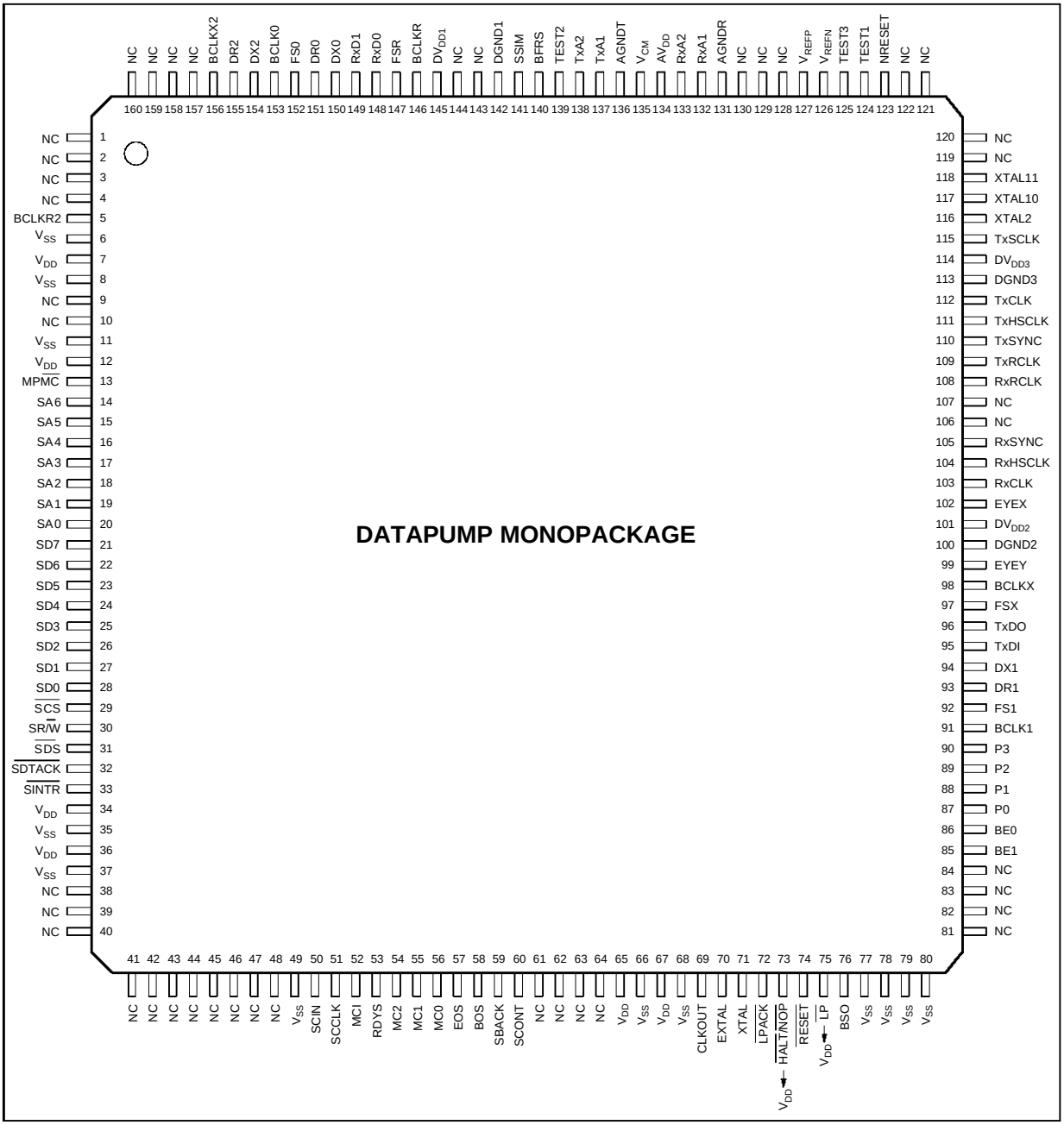


75C50-24.EPS

II.4 - ST18933PQFP Top View (PQFP160)



II.5 - ST75C50 Top View (PQFP160)



75C50-04.EPS

III - PIN DESCRIPTION

III.1 - Host Interface

The exchanges with the control processor proceed through a 64 Bytes DUAL port RAM shared between the DSP and the Host. The pins associated with this interface are :

Pin Name	Type	Description
SD0..SD7	I/O	System Data Bus. 8-bit data bus used for asynchronous exchanges between the DSP and the Host through the DUAL port RAM.
SA0..SA6	I	System address bus. 7-bit address bus for DUAL port RAM.
$\overline{\text{SDS}}$	I	System Data Strobe. Active low. Synchronizes all the exchanges.
SR/$\overline{\text{W}}$	I	System Read/Write
$\overline{\text{SCS}}$	I	System Chip Select. Active low
$\overline{\text{SDTACK}}$	O	System bus Data Acknowledge. Active low.
$\overline{\text{SINTR}}$	O	System Interrupt Request. Active low. This signal is asserted by the DSP and negated by the Host.
$\overline{\text{RESET}}$	I	Reset Active low
RING/BS0	I	Ring detect signal : awakens data-pump from its sleep mode.

III.2 - Serial Interface

The transmit and receive synchronous data exchanges between the DSP and microprocessor can pass via the Simplified Synchronous Serial Interface. Two pins are allowed for the data :

Pin Name	Type	Description
DR2	O	Synchronous Data Output
DX2	I	Synchronous Data Input

III.3 - Analog Interface

Pin Name	Type	Description
TXA1	O	Transmit Analog Output 1
TXA2	O	Transmit Analog Output 2
RXA1	I	Receive Analog Input 1
RXA2	I	Receive Analog Input 2
V_{CM}	I	Analog Common Voltage (nominal +2.5V)
V_{REFN}	O	Analog Negative Reference
V_{REFP}	O	Analog Positive Reference

III.4 - Eye Pattern Interface

A simplified dual 8-bit DAC is provided for eye pattern display.

Pin Name	Type	Description
EYEX	O	Analog Output for Constellation Display. (X AXIS)
EYEY	O	Analog Output for Constellation Display. (Y AXIS)

III.5 - Clock Interface

A complete set of bit and baud clocks are provided to allow the implementation of all the modem functions :

Pin Name	Type	Description
TxSCLK	I	Transmit Terminal Clock. This signal is used to synchronize the Transmit bit Clock with an external Transmit bit Clock. When not used this pin must be grounded or disabled by software
TxCLK	O	Transmit bit Clock
TxRCLK	O	Transmit Baud Clock. (Default 2400 Hz)
RxCLK	O	Receive bit Clock
RxRCLK	O	Receive Baud Clock. (Default value 2400 Hz)

In FSK mode TxCLK is 7200 Hz, RxCLK is 9600 Hz.

III.6 - Auxiliary Interface

A set of auxiliary signals are provided to simplify the DAA Interface. This is made by a three line General Purpose Parallel Input/Output.

Pin Name	Type	Description
PO	I/O	Parallel Input/Output 0
P1	I/O	Parallel Input/Output 1
P2	I/O	Parallel Input/Output 2

III.7 - Miscellaneous

Pin Name	Type	Description
XTAL	O	Internal oscillator Output. Left open if not used.
EXTAL	I	Internal oscillator Input, or External Clock
CLKOUT	0	EXTAL Divide by 2

Pin Name	Type	Description
XTAL10	I	MAFE oscillator input
XTAL11	I	MAFE oscillator input . Must be connected to XTAL10.
XTAL2	O	MAFE oscillator output

Note : The nominal external clock frequency of the DSP is 36.864MHz. The nominal external clock frequency of the MAFE is 18.432MHz with a precision better than $\pm 5.10^{-5}$ (and is output from the DSP on the CLKOUT Pin in the ST75C50 chipset).
When in Sleep Mode the CLKOUT clock is not available

III.8 - Interconnection

A set of signals is use for interconnection between the DSP and the Analog Front End. Refer to the corresponding appendix for the complete Electrical Schematics.

Pin Name		Description
DSP	**MAFE**	
P3	**NRESET**	Reset of the Analog Front End
BCLK0	**BCLKR**	Receive Serial I/O Clock
FS0	**FSR**	Receive Serial I/O Frame Synchro
DX0	**RXDI**	Receive Serial I/O Input
DR0	**RXDO**	Receive Serial I/O Output
BCLK1	**BCLKX**	Transmit Serial I/O Clock
FS1	**FSX**	Transmit Serial I/O Frame Synchro
DX1	**TXDI**	Transmit Serial I/O Input
DR1	**TXDO**	Transmit Serial I/O Output
BCLKX2	**RXCLK**	Receive Bit Clock
BCLKR2	**TXCLK**	Transmit Bit Clock
BE0	**RXRCLK**	Receive Baud Clock
BE1	**TXRCLK**	Transmit Baud Clock

Sections III. 9, 10 and 11 relate to the ST18933 for customer specific code.

III.9 - Memory Interface

A set of Digital signals is needed if using a 8K*8 (100ns access time) for Bulk Delay.

Pin Name	Type	Description
A0..A15	O	Address Bus (up to 64K)
D0..D15	I/O	Data Bus
$\overline{CS}$	O	Chip Select, Active when the DSP Access the Bulk Delay
$\overline{WR}$	O	Write, Active low
$\overline{RD}$	O	Read, Active low

III.10 - Boundary Scan Interface

A set of 13 signals are dedicated for Testing the DSP. These signals can be used in a development phase, associated with SGS-THOMSON ST18932 Boundary Scan Development Tools, to Debug the application Hardware and Software. If not used the corresponding input signals must be grounded.

Pin Name	Type	Description
SCIN	I	Scan Data Input
SCCLK	I	Scan Clock
SCOUT	O	Scan Data Output
BOS	I	Begin of Scan Control
EOS	I	End of Scan
MC0..MC2	I	Mode Control
SBACK	O	Software Breakpoint Acknowledge
MCI	O	Multicycle Instruction
RDYS	O	Ready to Scan Flag

III.11 - Open Version Interface

The ST18933 DSP 160 pin chip allows the use of an external program memory. This memory can be a ROM Memory (25ns access time) or a RAM Memory (25ns access time) that can be downloaded, via the DUAL Port Ram, by the host processor (refer to the ST18933 data sheet).

Pin Name	Type	Description
ID0..ID31	I/O	Instruction Data Bus
IA0..IA15	O	Instruction Address Bus
$\overline{EPM}$	O	Extenal Memory Select, Active low
$\overline{WPM}$	O	Extenal Memory Write, Active low
MP/$\overline{MC}$	I	Select Internal ROM Program (MP/MC = 0) or External ROM/RAM Program (MP/MC = 1)

IV. - ELECTRICAL SPECIFICATIONS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical value are given for V_{DD} = +5V and T_{amb} = 25°C and for nominal crystal frequency of 36.864 MHz.

IV.1 - Maximum Ratings (referenced to GND)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3, +7.0	V
V_I, V_{IN}	Digital or Analog Input Voltage	-0.3, V_{DD} + 0.3	V
I_I, I_{IN}	Digital or Analog Input Current	± 1	mA
I_O	Digital Output Current	± 20	mA
I_{OUT}	Analog Output Current	± 10	mA
T_A	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature (plastic)	-40, +125	°C
P_{tot}	Maximum Power Dissipation		mW

Stresses above those hereby listed may cause damage to the device. The ratings are stress related only and functional operation of the device in conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

IV.2 - DC Characteristics

V_{DD} = 5V ± 5%, GND = 0V, T_A = 0 to 70°C (Unless otherwise specified).

IV.2.1 POWER SUPPLY AND COMMON MODE VOLTAGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DD}	Supply Current		130		mA
I_{DD}-LP	Supply Current in Low Power Mode				mA
V_{CM}	Common Mode Voltage	V_{DD}/2 -5%	V_{DD}/2	V_{DD}/2 +5%	V

IV.2.2 - DIGITAL INTERFACE

All digital pins except XTAL pins.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage	-0.3		0.8	V
V_{IH}	High Level Input Voltage	2.2			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	0	+10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = 2mA)	2.8			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 2mA)			0.4	V
I_{OZ}	Three State Input Leakage Current (GND < V_O < V_{DD})	-50	0	50	µA
C_{IN}	Input Capacitance		5		pF

IV.2.3 - ANALOG INTERFACE

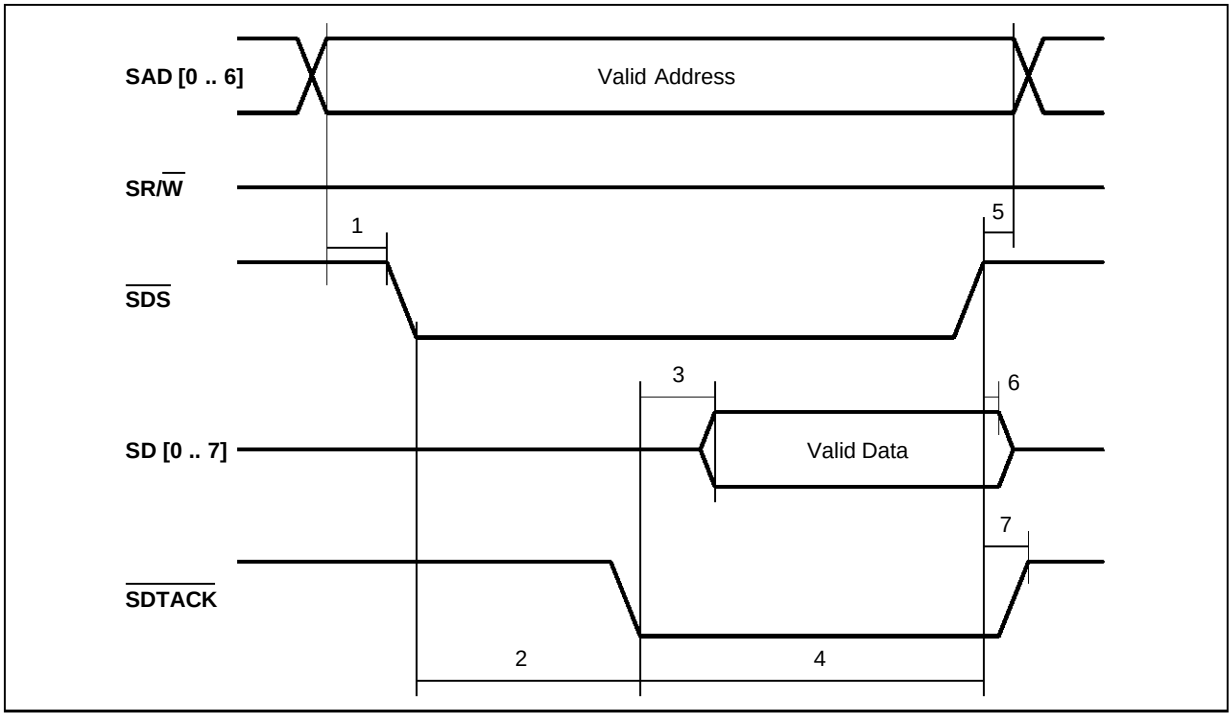
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{REF}	Differential Reference Voltage Output = V_{REFP} - V_{REFN}	2.40	2.50	2.60	V
Tempco	V_{REF} Temperature Coefficient		200		ppm /°C
V_{CMO-IN}	Input Common Mode Offset V = (RXA1+RXA2)/2 - V_{CM}	-300		300	mV
V_{DIF-IN}	Differential Input Voltage RXA1 - RXA2			2 Vref	Vpp
$V_{CMO-OUT}$	Output Common Mode Voltage Offset = (TXA1+TXA2)/2 - V_{CM}	200		200	mV
$V_{DIF-OUT}$	Differential Output Voltage TXA1 - TXA2			2 Vref	Vpp
$V_{OFF-OUT}$	Differential Output DC Offset (TXA1 - TXA2)	-100		100	mV

Symbol	Parameter		Min.	Typ.	Max.	Unit
Rin	Input resistance RXAx		100			kΩ
Rout	Output resistance	TXAx			20	Ω
		EYEx			50	kΩ
RL	Load resistance	TXAx	10			kΩ
		EYEx	1			MΩ
CL	Load capacitance	TXAx			50	pF
		EYEx			50	pF
Vout	Output voltage EYEx		GND		VDD	V

IV.3 - AC Electrical Characteristics

IV.3.1 - DUAL PORT RAM HOST READ-CYCLE TIMING

Figure 1

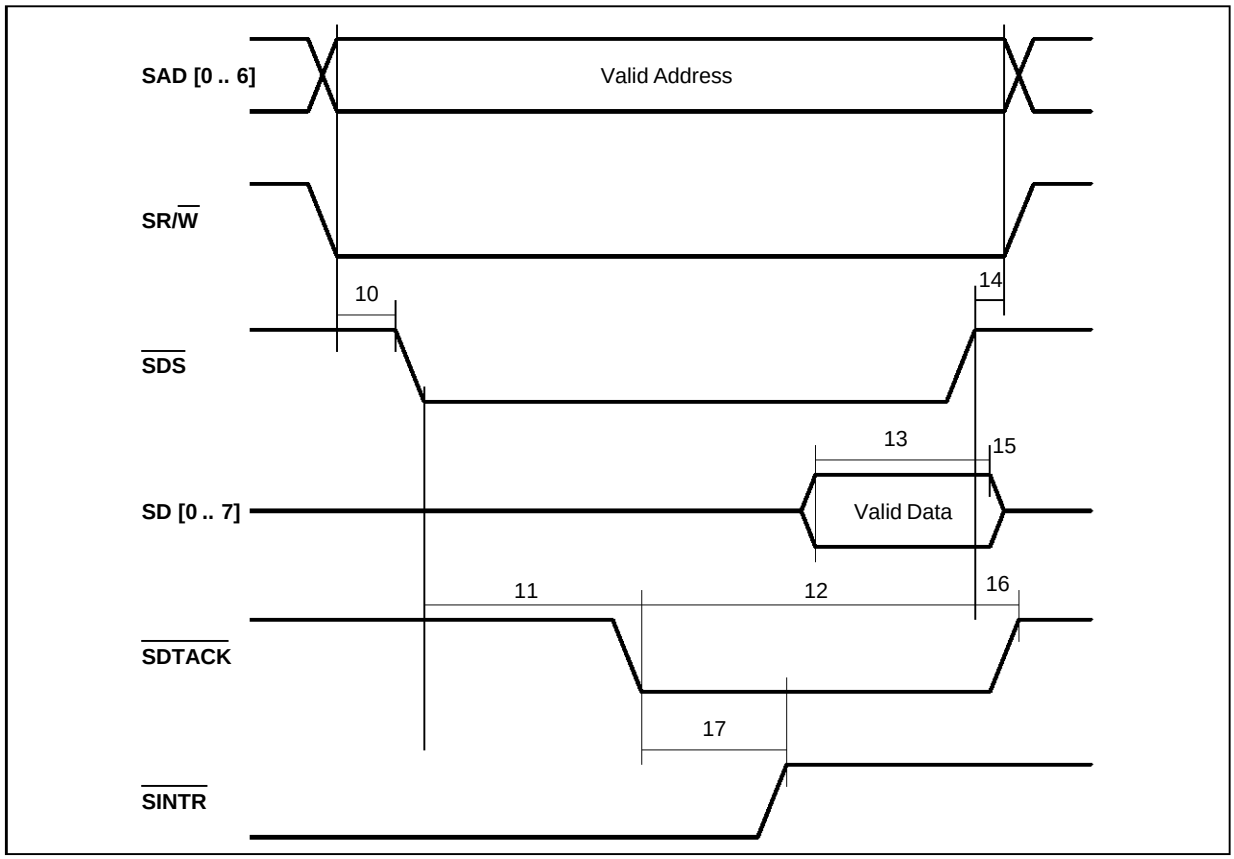


Number	Description	Min.	Typ.	Max.	Unit
1	Address, SR/W, SCS setup time	5			ns
2	SDTACK Acknowledge			235(1)	ns
3	SDTACK prepositionment time			30	ns
4	Data Strobe delay	50(2)			ns
5	Address Hold time	0			ns
6	Data Hold time	0			ns
7	SDTACK Hold time	0		10	ns

Notes : (1) this value is given for a DSP Cycle time of 56ns. For different Cycle Time t_c this value is $4 * t_c + 10$ ns.
(2) if the application does not use the SDTACK signal, the minimum SDS low state must be 300ns (or $5 * t_c$).

IV.3.2 - DUAL PORT RAM HOST WRITE-CYCLE TIMING

Figure 2



Number	Description	Min.	Typ.	Max.	Unit
10	Address, SR/W, SCS setup time	5			ns
11	SDTACK Acknowledge			235(1)	ns
12	Data Strobe Delay	50(2)			ns
13	Data Setup Time	10			ns
14	Address Hold time	0			ns
15	Data Hold time	0			ns
16	SDTACK Hold time	0		10	ns
17	SINTR Clear Delay	0		66(3)	ns

Notes : (1) this value is given for a DSP Cycle time of 56ns. For different Cycle Time t_c this value is $4 * t_c + 10$ ns.
(2) if the application does not use the SDTACK signal, the minimum SDS low state must be 300ns (or $5 * t_c$).
(3) the maximum value is t_c + 10ns.

V - FUNCTIONAL DESCRIPTION

V.1 - System Architecture

The system is based on a two-chip set. The first chip is the ST75C500 dedicated DSP handling all the signal processing routines for transmission, reception and echo cancellation on modem signals. It also holds the tone generators and detectors. Alternately the ST18933 DSP is available for customer specific operations. The second chip is the ST7543 delta-sigma MAFE, which performs the AD/DA conversions as well as the signal pre or post-filtering, and the sampling interpolation on the echo cancellation path.
The chip set allows the design of a complete V32bis data-pump without any external component. A versatile dual port RAM allows an easy interface with most popular micro-controllers.

V.2 - Chip Set Interconnect Circuitry

Please refer to appendix F for a detailed schematic of the chip set interconnect circuitry.

V.3 - Operation

V.3.1 - MODES
The modem implementation is fully compatible with many popular CCITT and Bell recommendations. The modulation can be either Trellis Coded Modulation (TCM) as in V.33 14400, 12000, V.32bis 14400, 12000, 9600, 7200, V.32 9600 bps rates, Quadrature Amplitude Modulation (QAM) as in V.32bis 4800, V.32 9600, 4800, V.22bis 2400, Differential Phase Shift Keying (DPSK) as in V.22 1200, Bell 212A 1200 bps rates, or Frequency Shift Keying (FSK) as in V.21, V.23 and Bell 103 modes. Both the bit rate and the trellis options are determined during the initial modem handshake sequence. V.29, V.27ter and V.17 are also available for FAX transmission. Other modes of operation include tone and DTMF detection or generation and speech mode.

V.3.2 - TRANSMITTER DESCRIPTION
The signal pulses are shaped in a dedicated filter combined with a compromise transmit equalizer suited for transmission over strongly distorted lines. 3 different compromise equalizers are available and can be selected by software. User defined transmit equalizers can be downloaded in the DSP RAM.

V.3.3 - ECHO CANCELLER DESCRIPTION
The echo canceller consists of a near end and a far end echo canceller. Both are fractionally spaced and achieve a high cancellation of the echo paths. The receive signal reconstruction is purely digital by virtue of the MAFE architecture. The far end echo requires either an external low cost 8kx8-100ns memory (for the customisable product STI8933), or the allocation of an equivalent amount of RAM in the controller memory space. It also sustains up to 10Hz of frequency offset on the far end echo path without degradation of performance.

V.3.4 - RECEIVER DESCRIPTION
The receiver section handles complex signals and uses a fractionally spaced complex equalizer. It is able to cope with distant modem frequency drifts up to 10^{-4} as specified in the CCITT recommendations. It also compensates for phase jitter at multiple and simultaneous frequencies.

V.3.5 - TONE GENERATOR DESCRIPTION
Four tones can be simultaneously generated by the ST75C50. The tones are determined by their frequencies and by the output amplitude level. A set of specific command is also available for DTMF generation (using two of the four generators available).

V.3.6 - TONE DETECTOR DESCRIPTION
16 tones can be simultaneously detected by the ST75C50. Each of the tones to be detected is defined by the coefficients of a 4th order programmable IIR. Detection thresholds are also programmable from -45dBm up to -10dBm.

V.3.7 - DTMF DETECTOR DESCRIPTION
A DTMF detector is included In the ST75C50, it permits detection of valid DTMF digits. A valid DTMF digit is defined as a dual tone with total power higher than -35dBm, duration greater than 40ms and differential amplitude within 8dB (positive or negative).

V.3.8 - VOICE MODE DESCRIPTION
The ST75C50 voice mode allows the implementation of enhanced telephony functions such as answering machines. Incoming samples from the line are PCM-A-law coded and are written into the dual port RAM. The outgoing samples are decompressed using the same A-law and are output to the telephone line.

V.3.9 - ANALOG LOOP BACK TEST MODE
In any transmission standard and any data format, the ST75C50 can be configured for analog loop back test.

V.3.10 - DIGITAL LOOP BACK TEST MODE
These loop back modes comply with the test loop 2 of the CCITT V.54 recommendation for V.32 and V.32 bis. For V.22 and V.22 bis the digital loop back modes comply with these recommendations.

V.3.11 - SLEEP POWER MODE
Sleep state can be entered using a host command. Activating the reset signal or ring interrupt will wake up the data-pump. When in sleep mode, the dual port RAM is unavailable and the clocks are disabled. When the pump wakes up it issues an interruption IT5 when ready to operate.

V.4 - Modem Interface

V.4.1 - ANALOG INTERFACE
The modem designer must provide a proper hybrid interface to the ST75C50. An example of hybrid design is given in appendix. The inputs and outputs of the MAFE are differential, thus achieving better noise immunity.

V.4.2 - HOST INTERFACE
The host interface is seen by the micro as a 64x8 RAM (Motorola bus), with additional registers accessible through an 7-bit address space. This RAM can be used for data transmission using the SERIAL command.

V.4.3 - MEMORY INTERFACE
In custom application using the STI8933 an external bus gives access to a 8Kx8 100ns RAM for Bulk delay storage. External total data space is 48K.

V.4.4 - AUXILIARY PARALLEL INTERFACE
The auxiliary parallel interface is a general purpose 3-bit parallel interface, which carries various signals, used by the controller and the analog part of the modem. Each pin can be independently programmed for input or output.

V.4.5 - AUXILIARY SERIAL INTERFACE
The auxilliary serial interface is a serial synchronous I/O, which carries the bit data flow. When required, asynchronous serial mode can be achieved by adding the TS7538 Async/Sync converter.

V.4.6 - EXE PATTERN CONVERTERS
The output from these two D to A converters provides direct display of the constellation.

VI - USER INTERFACE

VI.1 - Dual Port Ram Description

The dual port RAM is the standard interface between the controller and the ST75C50, for either commands or data. This memory is addressed through a 7-bit address bus. The locations from $00 to $3F are RAM locations, while locations from $40 to $50 are control registers dedicated to the interrupt handling.

Several functional area are defined in the dual port RAM ,namely :

- the command area,
- the report area,
- the status area,
- the bulk delay exchange area,
- the data buffer areas,

VI.1.1 - MAPPING

VI.1.1.1 - Command Area

The command area is located from $00 to $04. Address $00 holds the command byte COMSYS, and the four next locations hold the parameters COMPAR[0..3]. The command parameters must be entered before the command word is issued. Once the command has been entered, the command byte is reset and an acknowledge report is issued. A new command should not be issued before the acknowledge counter COMACK is incremented. The command exchange rate has a maximum of 2400 Hz.

VI.1.1.2 - Report Area
The report area is located from address $05 to address $07. Location $05 holds the acknowledge counter COMACK. Each time a command is acknowledged, the report bytes COMREP[0..1] (if any) are written by the ST75C50 into locations $06 and $07, and the content of COMACK is incremented. This counter allows an acurate monitoring of the command processing by the ST75C50.

VI.1.1.3 - Status Area
The status area is located from address $08 to $0A. The error status word SYSERR is located at address $08. This error status word is updated each time an error condition occurs. An optional interruption IT0 may be triggered as well in the case of an error condition. Location $09 and $0A holds the general status bytes STATUS[0..1]. The meaning of the bits depends of the mode of operation, and is described in Appendix B. The third byte at address $0B holds the Quality Monitor byte STAQUA.

VI.1.1.4 - Optional Status Area
The user can program (through the DOSR command) the three locations STAOPT[0..2] of the Optional Status Area ($0C to $0E) for the real time monitoring of four arbitrary memory locations.

VI.1.1.5 - Bulk Delay Exchange Area
This area is reserved for V.32 / V.32bis storage of Far End echo canceller symbols. Refer to Appendix H and application note.

This area has two sub-sections :a flagging section ($0F to $13) and a bulk data area ($14 to $1B).
Location $0F holds the bulk data buffer status SYMSTA. Locations $10 and $11 (resp. $12 and $13) contain a pointer to the bulk data buffer SY-

MADR[0..1] (resp. SYMADT[0..1]), in the controller space, which should receive (resp. send) the next group of 8 delayed symbols. The ST75C50 manages thus an area of 4k bytes in a circular addressing mode inside the controller memory space. The buffer SYMBUF[0..7] containing the symbols received or sent to the controller is located from $14 to $1B.

VI.1.1.6 - Data Buffer Area

The Data Buffer Area is shared by a Data Buffer Status Area (from $1C to $1F) and a Data Area (from $20 to $3F). The data area is made of two double 8-byte buffers. Each of the four buffers is attached to a Status byte. The meaning of the status byte depends on the selected mode.

VI.1.2 - INTERRUPTIONS

The controller can generate 7 interrupts to the ST75C50, and the ST75C50 can generate 7 interrupts for the controller. The interrupt handling is made with a set of registers located from $40 to $50.
The interruptions generated by the ST75C50 come from seven different sources. Once the ST75C50 rises an interrupt, a signal is sent to the controller. The controller has then to process the interrupt and clear it. The interrupt source can be examined in the Interrupt Source Register ITSCRC located at $50. According to this status byte, the interrupt source can be determined. Then, writing at one of the memory location $40 to $46 (Reset Interrupt Registers ITREST[0..6]) will reset the corresponding interrupt (and thus acknowledge it). These seven sources of interruptions can be masked globally or individually using the Interrupt Mask Register ITMASK located at $4F.

The 7 series interrupt sources are :

IT0 Error/Warning : an error has occurred and the error code is available in the error status byte SYSERR. This byte can be selectively cleared by the CSE command.

IT1 Bulk Delay : the bulk delay buffer requires an action from the controller, for emptying it and for filling it with symbols.

IT2 Tx Buffer : each time the ST75C50 frees a buffer, this interrupt is generated.

IT3 Rx Buffer : each time the ST75C50 has filled a buffer, this interrupt is generated.

IT4 Status Byte : the modem status byte has changed and has to be checked by the controller.

IT5 Power Down Mode : the ST75C50 has been awakened by a low level on the BS0/RING Pin. The host has to reset the ST75C50 by the RESET signal.

IT6 Command Acknowledge : the ST75C50 has read the last command entered by the host, incremented the command counter COMACK, and is ready for a new command.

VI.1.3 - HOST INTERFACE SUMMARY

Address (hex)	Description	Size (Byte)	Mnemonic
COMMAND AREA			
$00	Command	1	COMSYS
$01-$04	Command Parameters	4	COMPAR[0..3]
REPORT AREA			
$05	Acknowledge Counter	1	COMACK
$06-$07	Report	2	COMREP[0..1]
STATUS AREA			
$08	Error Status	1	SYSERR
$09	General Status	2	STATUS[0..1]
$0B	Quality Monitor	1	STAQUA
$0C-$0E	Optional Report	3	STAOPT[0..2]
BULK DELAY AREA			
$OF	Symbol Buffer Status	1	SYMSTA
$10-$11	Symbol Rx Buffer Pointer	2	SYMADR[0..1]
$12-$13	Symbol Tx Buffer Pointer	2	SYMADT[0..1]
$14-$1B	Symbol Buffer	8	SYMBUF[0..7]
DATA AREA			
$1C	Data Rx Buffer 0 Status	1	DTRBS0
$25	Data Rx Buffer 1 Status	1	DTRBS1
$2E	Data Tx Buffer 0 Status	1	DTTBS0
$37	Data Tx Buffer 1 Status	1	DTTBS1
$1D-$24	Data Rx Buffer 0	8	DTRBF0[0..7]
$26-$2D	Data Rx Buffer 1	8	DTRBF1[0..7]
$2F-$36	Data Tx Buffer 0	8	DTTBF0[0..7]
$38-$3F	Data Tx Buffer 1	8	DTTBF1[0..7]
INTERRUPT AREA			
$40-$46	Reset Interrupt Register	7	ITREST[0..6]
$4F	Interrupt Mask Registe	1	ITMASK
$50	Interrupt Source Register	1	ITSRCR

VI.2 - Command Set

The Command Set has the following attractive features :

- user friendly with easy to remember mnemonics.
- possibility of straight forward expansion with new commands to suit specific customer requirements.
- easy upgrade of existing software using previous modem based SGS-THOMSON products.

The command set has been designed to provide the necessary functional control on the ST75C50. Each command is classified according to its syntax and the presence/absence of parameters. In the case of a parametric command, parameters must first be written into the dual port RAM before the command is issued. Acknowledge and error report is issued for each command entered.

VI.2.1 - COMMAND SET SUMMARY

VI.2.1.1 - Operational Control Commands

INIT Initialize. Initialize the modem chipset. Set all parameters to their default values and wait for commands of the control processor. Non parametric command.

IDT Identify. Return the product identification code. Non parametric command.

SLEEP Turn to Sleep Power Mode. The modem engine issues a control signal to the MAFE in order to switch to Sleep Power Mode, then switches itself into Sleep Power Mode. Non parametric command.

HSHK Handshake. Begins the handshake sequence. The modem chipset carries all the steps defined in the CCITT recommendations. A status report indicates to the control processor the state of the handshake and the final negotiated transmission bit rate. This command only applies to modes where a handshake sequence is defined. A CONF command must have been issued prior to the use of HSHK. Non parametric command.

RTRA Retrain. Start sending the retrain sequence as specified in the CCITT recommendation. This command only applies to modes where a retrain sequence is defined. In V.32bis, this command also initiates the rate negotiation sequence. Parametric command.

CSE Clear Status Error. Selectively clears the Error status byte SYSERR. Parametric command.

SETGN Set gain. This command sets the global gain factor, which is used for the transmit samples. Parametric command.

STOP FAX Stop. Stop FAX half duplex transmitter. Non parametric command.

SYNC FAX Synchronize. Start/Stop of FAX half duplex receiver. Parametric command.

VI.2.1.2 - Data Communication Commands

XMIT Transmit data. Enable/disables the transmission of data. After a XMIT command, according to the selected mode (either serial or parallel), the ST75C50 sends the data contained either in its dual port RAM or fed through the serial I/O. Parametric command.

SERIAL Enables/disables the Data Serial Mode. This command selects the data source, i.e. either parallel or serial. The parallel mode uses a part of the dual port RAM as a double buffer. The serial mode uses the serial synchronous I/O. Parametric command.

VI.2.1.3 - Digital Loop Back Commands

V54 V.54 Digital Loop Back. Enables/Disables the transmission and reception of V.54 patterns. This command must be used only in V.32 bis or V.32 mode. Parametric command.

V22L2 V.22/V.22 bis Digital Loop Back. Enables/Disables the transmission and reception of V.22 Loop 2 patterns. This command must be used only in V.22 bis or V.22 mode. Parametric command.

VI.2.1.4 - Memory Handling Commands

MW Memory Write. This command is used to write an arbitrary 16-bit value into the writable memory location currently specified by a parameter. Parametric command.

MR Memory Read. This command allows the controller to read any of the ERAM or CROM (internal and external DSP memory spaces) locations without interrupting the processor. Parametric command.

CR Complex Read. This command allows the controller to read at the same time the real and imaginary part of a complex value stored in a double ERAM or CROM location. This feature is very interesting for eye pattern software control as well as for equalization monitoring. This command insures that the real and imaginary part are sampled in the memory at the same time (integrity). Parametric command.

VI. 2.1.5 - Configuration Control Commands

CONF Configures. This command configures the modem chipset for data transmission and handshake procedures (if any) in any of the supported modes. The transmission parameters are set to their default values and can be modified with the MODC command. This command also defines the parameters in the case of an automatic standard recognition and the boundaries of the speed negotiation. Parametric command.

MODC Modify Configuration. This command allows modification of part of the parameters set up by the CONF command. Parametric command.

BULK Define Symbol Bulk Management. This command selects the dual port RAM symbol management, allowing removal of all external RAM directly connected to the DSP. Parametric command.

DOSR Define Optional Status report. This command allow the modification of the optional status report located in the status area of the dual port RAM. One can thus select a particular parameter to be monitored during all modes of operation. Parametric command.

DSIT Define Status Interrupt. This command allows the programmation of the status word bit that will generate an Interrupt to the controller. Parametric command.

PPS Parallel Port Set. This command allows the modification of the parallel port configuration. Each of the four bits of this port can be programmed either as an input or an output. Parametric command.

PPR Parallel Port Read. This command reads the value of the 4-bit parallel port. The value is read whether it is an input or not. Non parametric command.

PPW Parallel Port Write. This command writes a 4-bit value into the parallel port. The bits are masked according to their input/output status. Parametric command.

VI.2.1.6 - MAFE Control Commands

WMR Write MAFE register. Causes the DSP to write a parameter into a MAFE register. Parametric command.

VI.2.1.7 - Tone Generation Commands

TONE Select Tone. Programs the tone generator(s) for the desired default tone(s). Additional mnemonics provide quick programming of DTMF tones or other currently used tones. Parametric command.

DEFT Define Tone. Programs the tone generator(s) for arbitrary tone synthesis. Parametric command.

TGEN Tone Generator Control. Enables or disables the tone generator(s). Parametric command.

IV.2.1.8 Tone Detection Commands

TDRC Read coefficients of tone detection cell. Parametric command.

TDWC Write coefficients of tone detection cell. Parametric command.

TDRW Read wiring of tone detection cell. Parametric command.

TDWW Write wiring to tone detection cell. Parametric command.

TDZ Clear the values of tone detection cell. Parametric command.

VI.2.2 - COMMAND SET SHORT FORM

Mnemonic	Value	planation
INIT	0X06	**INIT**ialization
IDT	0X14	**ID**en**T**ify
SLEEP	0X03	**SLEEP** mode
HSHK	0X04	**H**and**SH**a**K**e
RTRA	0X05	**R**e**TRA**in
CSE	0X08	**C**lear **S**tatus **E**rror
SETGN	0X02	**SET G**ai**N**
XMIT	0X01	**R**eceive/**T**rans**MIT** data
SERIAL	0X07	**SERIAL** mode
MW	0X12	**M**emory **W**rite
MR	0X10	**M**emory **R**ead
CR	0X11	**C**omplex **R**ead
CONF	0X20	**CONF**igure
MODC	0X21	**MOD**ify **C**onfiguration
BULK	0X22	Define symbol **BULK** management
DOSR	0X0A	**D**efine **O**ptional **S**tatus **R**eport
DSIT	0X13	**D**efine **S**tatus word **I**n**T**errupt
PPS	0X15	**P**arallel **P**ort **S**et
PPR	0X16	**P**arallel **P**ort **R**ead
PPW	0X17	**P**arallel **P**ort **W**rite
WMR	0X0B	Write **M**afe **R**egister
TONE	0X0C	select **TONE**
DEFT	0X0E	**DEF**ine **T**one
TGEN	0X0D	**T**one **GEN**erator control
TDRC	0X1A	**T**one **D**etect **R**ead **C**oefficient
TDWC	0X1C	**T**one **D**etect **W**rite **C**oefficient
TDRW	0X1B	**T**one **D**etect **R**ead **W**iring
TDWW	0X1D	Tone **D**etect **W**rite **W**iring
TDZ	0X1E	**T**one **D**etect **Z**ero cell
V54	0X23	Enable/Disable **V**.**54**
V22L2	0X24	Enable/Disable **V**.**22 L**oop**2**
STOP	0X25	FAX **STOP** Transmitter
SYNC	0X26	FAX **SYNC**hronize Receiver

VI.2.2.1 - Miscellaneous Commands
(for ST18933 with Custom Code)

CALL Call a Subroutine. Call a Subroutine with one parameter.

JSR Call a low level Subroutine. Call an internal subroutine with one parameter.

VI.3 - Status - Reports

VI.3.1 - STATUS

The ST75C50 has a dedicated status reporting area located in its dual port RAM. This allows a continuous monitoring of the status variables without interrupting the DSP.

The first status byte gives the error status. Issuing of an error status can be also flagged by a maskable interrupt for the controller. The signification of the error codes is given in Annexe B.

The second and third status bytes give the general status of the modem. This two byte status can generate, when a change occurs, an interrupt to the controller; each bit of that two byte word can be masked independently.

The fourth byte gives, in real time, a measure of the reception quality. This information may be used by the controller for retrain purpose.

Three other locations are dedicated for custom status reporting. This status includes, for example, the handshake phase, the negotiated data rate, and other items described in Annexe B. The controller can program the ST75C50 for a real time monitoring of any of its internal RAM location. High byte or low byte of any word can thus be monitored.

VI.3.2 - REPORTS

The ST75C50 features an acknowledge and report facility. The acknowledge of a command is monitored by a counter COMACK located in the dual port RAM. Each time a command is executed from the command area, the ST75C50 will increment this counter. For instance, when a MR (Memory Read) command is issued, the data is first written in the report area, and the counter is incremented afterwards. This way of processing insures the data integrity as well as an additional synchronization between the controller and the data pump.

V.4 - Data Exchanges

The ST75C50 accepts two kinds of data exchanges : Parallel synchonous through the DUAL RAM or SERIAL synchronous. Detailed description of the Data Buffer Exchange modes of operation is available in Annex G.

VI.4.1 - PARALLEL DATA MODE

VI.4.1.1 - Transmit

The controller must first fill at least the first buffer of data (Tx Buffer 0) with the bits to be transmitted. In order to perform this operation, the controller must first check the Tx Buffer 0 status word DTTBS0. If this buffer is empty, the controller fills the data buffer locations (up to 64 bits), and then writes in DTTBS0 the number of bits contained in the buffer. The controller can then either proceed with the second buffer or initiate the transmission with a XMIT command.

The ST75C50 copies the contents of the data buffer and then clears the buffer status word in order to make it again available. The number of bits specified by the status word is then queued for transmission. The process goes on with the two buffers until an XMIT command stops the transmission. After the finishing XMIT command has been issued, the last buffers are emptied by the ST75C50.

Error occurs when both buffers are empty while the transmit bit queue is also empty. Error is signalled with an interruption to the controller through the SYSERR register.

VI.4.1.2 - Receive

The controller should take care of releasing the Rx buffers before the Data Carrier Detect goes true. This is made by writing the correct status word in the Rx Buffer Status 0 and 1. The ST75C50 then fills the first buffer, and once filled sets the status word with the number of bits received. It then takes control of the second buffer and operates in the same way. The controller must check the status of the buffers and empty them. Once the data is read, the controller must release the used buffer and wait for the next buffer to be full. Interrupts are available for an additional flagging of these events.
Error occurs when both buffers are declared full, and incoming bits still arrive from the line.
Synchronous Data Buffer Exchanges are described in Annex H.

VI.4.3 - SERIAL EXCHANGES

The second mode of operation for data exchanges is the Serial Synchronous Mode. In this mode, the data I/O is made through a pair of dedicated hardware pins. Asynchronous mode of operation and full implementation of the V.14 recommendation can be achieved with the use of the TS7538 Async/sync converter.

APPENDIX A : COMMAND SET DESCRIPTION

Commands are presented according to the following form :

COMMAND - Command name meaning

Opcode : hexadecimal digit

X	X	X	X	X	X	X	X

Synopsis

Short description of the functions performed by the command

Parameters

Field	Byte	Pos.	Value	Definition
Name	X	a..b		Explanation of the parameter
			xx *	Default value

Field : Name of the addressed bit field.
Byte : Index (or address in the dual port RAM) of the parameter byte (from 1 to 4).
Pos. : Bit field position inside the parameter byte. Can either be a single position (from 0 to 7, 0 being LSB) or a range.
Value : Possible values for the bit (resp. bit field). *range* means all values are allowded. A value preceded by a star means a default value. Values are expressed either under the form of a bit string, or under hexadecimal format.

Command :

BULK - Enable Symbol Management

Opcode : 22

0	0	1	0	0	0	1	0

Synopsis

BULK allows the use of the DUAL RAM symbol area. This additional task into host firmware is only needed in V.32/V.32bis mode. Using this command allows the removal of all external RAM connected to the DSP local bus. This mode of operation is mandatory with the single chip ST75C50 package and 80 pin package.

In this command the user sets the virtual memory base address and the top memory address (the base address must be on a 8 byte boudary and the top address on a 8 byte boudary - 1 eg : 0x67FF).

Parameters

Field	Byte	Pos.	Value	Definition
BA_ADDR_L	1	0..7		Low byte of the base address
BA_ADDR_H	2	0..7		High byte of the base address
TO_ADDR_L	3	0..7		Low byte of the top memory address
TO_ADDR_H	4	0..7		High byte of the top memory address

CALL - Call a subroutine

Opcode : 19

0	0	0	1	1	0	0	1

Synopis

For use with custom code in the STI8933 only

CALL allows to execute a part of the DSP firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	0..7		Low byte of the call address
C_ADDR_H	2	0..7		High byte of the call address
C_DATA_L	3	0..7		Low byte of the argument
C_DATA_H	4	0..7		High byte of the argument

CONF - Configure for operations

Opcode : 20

0	0	1	0	0	0	0	0

Synopsis

CONF allows the complete definition of the modem operation. It also defines the speed boundaries in the case of a negotiated rate.

Parameters

Field	Byte	Pos.	Value	Definition
CONF_TX	1	1..0	00* 01 10 11	DTMF Tone reserved Audio : transmit speech signal Modem : transmit data signal
CONF_RX	1	3..2	00* 01 10 11	Tone detection DTMF detection Audio : receive speech signal Modem : receive data signal
CONF_ALOO P	1	4	0 1	normal mode Analog loop back mode
CONF_PSTN	1	5	0 1	PSTN Leased line
CONF_AO	1	6	0 1	Answer mode Originate mode

Parameters (continued)

Field	Byte	Pos.	Value	Definition
CONF_MODE	2	5..0	0 1 2 3 4 5 6 7 8 9 A B C	Automode Bell 103 Bell 212A V.21 V.23 V.22 V.22bis V.27ter V.29 V.17 V.32 V.32bis V.33
CONF_TX EQ	2	7..6	00 01 10 11	Flat Tx equalizer TX equalizer #1 (1/2 of M1020) Tx equalizer #2 (1/2 of M1040) Reserved
CONF_QAM	3	0	0 1	QAM/DPSK only (Automode) FSK allowed (Automode)
CONF_TCM	3	1	0 1	Trellis coding not allowed Trellis coding allowed
CONF_300	3	2	0 1	300 bps speed not allowed 300 bps speed allowed
CONF_1200	3	4	0 1	1200 bps speed not allowed 1200 bps speed allowed
CONF_2400	3	5	0 1	2400 bps speed not allowed 2400 bps speed allowed
CONF_4800	3	6	0 1	4800 bps speed not allowed 4800 bps speed allowed
CONF_7200	3	7	0 1	7200 bps speed not allowed 7200 bps speed allowed
CONF_9600	4	0	0 1	9600 bps speed not allowed 9600 bps speed allowed
CONF_12000	4	1	0 1	12000 bps speed not allowed 12000 bps speed allowed
CONF_14400	4	2	0 1	14400 bps speed not allowed 14400 bps speed allowed

Notes : 1) When receiving the **CONF** command the modem will reset all the **MODC** parameters to their default values.

2) The valid combinations of **CONF_TX** and **CONF_RX** are defined in the following table, associated with the number of tone detector cells running at the same time:

RX / TX	TONE/DTMF	MODEM	AUDIO
TONE	16	not allowed	16
DTMF	4	not allowed	4
MODEM	not allowed	2	not allowed
AUDIO	16	not allowed	16

When in modem mode the number of tone detectors allowed is set to 2 if using the SERIAL link and 0 if using the parallel data management (either Tx or Rx).

CR - Complex read

Opcode : 11

0	0	0	1	0	0	0	1

Synopsis

CR allows the reading of a complex parameter. The parameter specifies the parameter address (for the real part : the imaginary part is next location). CR returns the high byte value of both real and imaginary part of the addressed complex parameter.

Parameters

Field	Byte	Pos.	Value	Definition
CR_ADDR_L	1	7..0		Low byte of the 16-bit address
CR_ADDR_H	2	7..0		High byte of the 16-bit address

CSE - Clear error status

Opcode : 08

0	0	0	0	1	0	0	0

Synopsis

CSE is used to clear the ST75C50 error status SYSERR byte. It is also used as an acknowledge to the error condition handler.

Parameters

Field	Byte	Pos.	Value	Definition
ERR_MASK	1	0..7		Error mask . See report appendix for detailed meaning.

DEFT - Define arbitrary tone

Opcode : 0E

0	0	0	0	1	1	1	0

Synopsis

DEFT programs one of the four tone generator for arbitrary tone generation. The parameter is the frequency of the generated tone in Hertz between 0 and 3600 Hz (expressed in hexadecimal). Frequency above the half of the transmit sampling clock will be aliased.

Parameters : Example 1000 Hz is represented by 03E8

Field	Byte	Pos.	Value	Definition
TONE_GEN_SL	1	1..0		Index of the tone generator (0..3)
TONE_FREQ_L	2	7..0		Low byte of the frequency
TONE_FREQ_H	3	7..0		High byte of the frequency (internally masked with 0F)
TONE_SCALE	4	7..0		Amplitude scaling factor (high byte) FF gives the Maximum Amplitude.

DOSR - Define optional status report

Opcode : 0A

0	0	0	0	1	0	1	0

Synopsis

DOSR specifies the address of the parameters to be monitored in the 3 locations STAOPT[0..2] of the dual port RAM. It also specifies the assignment of the parameter inside the 3 locations.

Parameters

Field	Byte	Pos.	Value	Definition
STA_OPT_ASS	1	0..2		Index of the STAOPT array
STA_OPT_ADL	2	0..7		Low byte of parameter address
STA_OPT_ADH	3	0..3		High byte of parameter address
STA_OPT_HL	3	7	0 1	Select low byte of parameter Select high byte of parameter

DSIT - Define status interrupt

Opcode : 13

0	0	0	1	0	0	1	1

Synopsis

DSIT specifies the bit mask used with the **STATUS[0]** or **STATUS[1]** byte to generate an interrupt **IT4** to controller. Each time a bit change will append in the general status words, assuming the corresponding bit mask will be set, an interrupt will be generated.

Parameters

Field	Byte	Pos.	Value	Definition
STA_IT_MSK0	1	0..7		Select status word 0 Bit Mask pattern
STA_IT_MSK1	2	0..7		Select Status word 1 Bit Mask pattern

Note : The default IT status is 0X3F for STATUS [0] and 0XFF for STATUS [1].

HSHK - Handshake

Opcode : 04

0	0	0	0	0	1	0	0

Synopsis

HSHK is used to command the ST75C50 to begin the handshake sequence processing. The progress of the handshake is reported to the control processor.

Parameters : non parametric command

IDT - Identify

Opcode : 14

0	0	0	1	0	1	0	0

Synopsis

IDT returns the ST75C50 Harware and Software release number.

Parameters : non parametric command

Bits 15 to 12 represent the product identity number. For the 75C50 this is 0
Bits 11 to 4 represent the product software release
Bits 3 to 0 represent the software sub release

INIT - Initialization

Opcode : 06

0	0	0	0	0	1	1	0

Synopsis

INIT forces the ST75C50 to reset all parameters to their default conditions and restart operations.

Parameters : non parametric command

Note: This command makes a software reset of the ST75C50 and so cannot have the regular handshake protocol. It does not increment the COMACK, nor generate an Interrupt.

JSR - Call a low level subroutine

(For use with custom code in the STI8933 only)

Opcode : 18

0	0	0	1	1	0	0	0

Synopsis

JSR allows execution of DSP firmware with specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	0..7		Low byte of the call address
C_ADDR_H	2	0..7		High byte of the call address
C_DATA_L	3	0..7		Low byte of the argument
C_DATA_H	4	0..7		High byte of the argument

MR - Memory read

Opcode : 10

0	0	0	1	0	0	0	0

Synopsis

MR allows the reading of a 16-bit parameter. The parameter specifies the parameter address.

Parameters

Field	Byte	Pos.	Value	Definition
MR_ADDR_L	1	7..0		Low byte of the 16-bit address
MR_ADDR_H	2	7..0		High byte of the 16-bit address

MODC - Modify configuration

Opcode : 21

0	0	1	0	0	0	0	1

Synopsis

MODC allows modification of the configuration for special purposes. This command can also apply when in data mode.

Parameters

Field	Byte	Pos.	Value	Definition
MODC_V22G	2	3..4	00* 01 10	No guard tone 1800 Hz guard tone 550 Hz guard tone
MODC_FPT	2	2..3	00* 10	No echo protection tone (FAX only) V29, V27, V33, V17 Long echo protection tone (180ms)
MODC_NOT A	2	4	0*	Generate answer tone for handshake (ANSWER MODE) Wait answer tone (ORIGINATE MODE)
	2	4	1	Do not wait answer tone (ORIGINATE MODE) Do not generate answer tone (ANSWER MODE)
MODC_NOSA	2	6	0* 1	Cut answer tone when receiving AA (V.32b) Continue answer tone
MODC_NOQA	2	7	0* 1	Enable V.32 bis handshake on quality Disable handshake on quality

MW - Memory write

Opcode : 12

0	0	0	1	0	0	1	0

Synopsis

MW allows the writing of a 16-bit parameter. The parameter specifies the address, as well as the value, to be transferred.

Parameters

Field	Byte	Pos.	Value	Definition
MW_ADDR_L	1	7..0		Low byte of the 16-bit address
MW_ADDR_H	2	7..0		High byte of the 16-bit address
MW_VALUE_L	3	7..0		Low byte of the 16-bit value
MW_VALUE_H	4	7..0		High byte of the 16-bit value

PPR - Read parallel port

Opcode : 16

0	0	0	1	0	1	1	0

Synopsis

Read parallel port. The values of the 4-bit parallel port is read, whether the port is configured in input or in output.

Parameters : non parametric command

PPS - Parallel port set

Opcode : 15

0	0	0	1	0	1	0	1

Synopsis

Configure parallel port. Each of the 4 pins of the parallel port can be either programmed for input or for output.

Parameters

Field	Byte	Pos.	Value	Definition
PP_IO0	1	0	0* 1	Pin 0 programmed as input Pin 0 programmed as output
PP_IO1	1	1	0* 1	Pin 1 programmed as input Pin 1 programmed as output
PP_IO2	1	2	0* 1	Pin 2 programmed as input Pin 2 programmed as output
PP_IO3	1	3	0 1*	Pin 3 programmed as input Pin 3 programmed as output

Note: Pin 3 is reserved for MAFE control and therefore must be programmed as an output.

PPW - Parallel port write

Opcode : 17

0	0	0	1	0	1	1	1

Synopsis

Write to the parallel port. This operation will be effective only if the bits are programmed as outputs.

Parameters

Field	Byte	Pos.	Value	Definition
PP_VAL0	1	0		Pin 0 logical value
PP_VAL1	1	1		Pin 1 logical value
PP_VAL2	1	2		Pin 2 logical value
PP_VAL3	1	3	1	Pin 3 logical value must be set to 1

RTRA - Retrain

Opcode : 05

0	0	0	0	0	1	0	1

Synopsis

RTRA is used to force the ST75C50 to initiate a retrain sequence on the channel. The parameter determines the target speed for the retrain.

Parameters

Field	Byte	Pos.	Value	Definition
RTRA_NEGO	1	0	0 1	Retrain (V.22bis, V.32, V.32bis) Rate Negotiation (V.22bis, V.32bis)
RTRA_NEGO	1	1	1 0	Trellis coding enabled Trellis coding not enabled
RTRA_1200	1	4	0 1	1200 bps speed not allowed 1200 bps speed allowed
RTRA_2400	1	5	0 1	2400 bps speed not allowed 2400 bps speed allowed
RTRA_4800	1	6	0 1	4800 bps speed not allowed 4800 bps speed allowed
RTRA_7200	1	7	0 1	7200 bps speed not allowed 7200 bps speed allowed
RTRA_9600	2	0	0 1	9600 bps speed not allowed 9600 bps speed allowed
RTRA_12000	2	1	0 1	12000 bps speed not allowed 12000 bps speed allowed
RTRA_14400	2	2	0 1	14400 bps speed not allowed 14400 bps speed allowed

SERIAL - Select serial or parallel mode

Opcode : 07

0	0	0	0	0	1	1	1

Synopsis

SERIAL defines the data path, i.e. either serial or parallel.

Parameters

Field	Byte	Pos.	Value	Definition
TX_SDATA	1	0	0* 1	Use parallel link for Tx data Use serial link for Tx data
RX_SDATA	1	1	0* 1	Use only serial link for Rx data Use also parallel link for Rx data

Note : The received bits always go to output pin DX2, even when the Rx_SDATA bit is set.

SETGN - Set output gain

Opcode : 02

0	0	0	0	0	0	1	0

Synopsis

SETGN is a command which sets the scaling factor of the transmit samples. It is used for setting the output level or for setting the level of the tone generators. The gain value is given in the form of a 2's complement 16-bit value.

eg :	7FFF	0dB
	4000	-6dB
	2000	-12 dB
	0	mute

Parameters

Field	Byte	Pos.	Value	Definition
GAIN_L	1	7..0	range FF*	Low byte of the 16-bit gain value
GAIN_H	2	7..0	range 7F*	Hight byte of the 16-bit gain value

SLEEP - Turn to sleep mode

Opcode : 03

0	0	0	0	0	0	1	1

Synopsis

SLEEP is used to force the ST75C50 to turn to sleep mode.

Parameters : non parametric command

Note: When receiving this command the ST75C50 will stop processing and so cannot have the regular handshake protocol. It does not increment the COMACK, nor generate an Interrupt. A negative level on the RING Pin will awaken the ST75C50, generate an IT5 Power Down Interrupt and execute a Software Reset (idem init).

STOP - FAX stop transmitter

Opcode : 25

0	0	1	0	0	1	0	1

Synopsis

STOP is used, in FAX modes, to force the ST75C50 to turn-off the transmitter in accordance with the corresponding CCITT V33/V17/V29/V27 recommendation.

Parameters : non parametric command

Note: When receiving this command the ST75C50 will stop sending regular data. In parallel mode this command must be preceded by a **XMIT** stop command. After receiving the **STOP** command the ST75C50 will wait until all the transmit buffers are sent commencing with the stop sequence.

SYNC - FAX synchronize the receiver

Opcode : 26

0	0	1	0	0	1	1	0

Synopsis

SYNC is used, in FAX modes, to force the ST75C50 to start/stop the receiver in accordance with the corresponding CCITT V33/V17/V29/V27 recommendation.

As soon as the ST75C50 receives the **SYNC** start command it sets its receiver to detect the FAX synchronization signal.

This commdand is the equivalent **HSHK** command for the receiver.

Parameters

Field	Byte	Pos.	Value	Definition
RX_SYNC	1	0	0* 1	Stop receiver Start receiver synchronization

TDRC - Tone detector read coefficient

Opcode : 1A

0	0	0	1	1	0	1	0

Synopsis

TDRC read one coefficient of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	0..3	0..F	Tone detector cell number
TD_C_ADDR	2	0..7	0..B 10 20 other	Biquad coefficient Energy coefficient Static level Reserved

The command answer is : low byte of coefficient followed by high byte of coefficient

TDRW - Tone detector read wiring

Opcode : 1B

0	0	0	1	1	0	1	1

Synopsis

TDRW read wiring of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	0..3	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1 other	Biquad and energy input Comparator inputs Reserved

The command answer is :

a) if TD_W_ADDR = 0 :
- first byte is the node number of signal connected to biquadratic filter input,
- second byte is the node number of the signal connected to the energy estimator input.

b) if TD_W_ADDR = 1 :
- first byte is the node number of signal connected to comparator negative input,
- second byte is the node number of the signal connected to the comparator positive input.

TDWC - Tone detector write coefficient

Opcode : 1C

0	0	0	1	1	1	0	0

Synopsis

TDWC write one coefficient of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	0..3	0..F	Tone detector cell number
TD_C_ADDR	2	0..7	0..B 10 20	Biquad coefficient Energy coefficient Static level
TD_COEFL	3	0..7		Low byte of coefficient
TD_COEFH	4	0..7		High byte of coefficient

TDWW - Tone detector write wiring

Opcode : 1D

0	0	0	1	1	1	0	1

Synopsis

TDWW write wiring of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	0..3	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1	Biquad and energy input Comparator inputs

if TD_W_ADDR = 0 (select biquad and energy inputs)

Field	Byte	Pos.	Value	Definition
TD_W_ERN	3		0..3F	Energy estimator signal input
TD_W_BIQ	4		0..3F	Biquad filter signal input

if TD_W_ADDR = 1 (select comparator inputs)

Field	Byte	Pos.	Value	Definition
TD_W_CN	3		0..3F	Negative comparator signal input
TD_W_CP	4		0..3F	Positive comparator signal input

TDZ - Tone detector clear cell

Opcode : 1E

0	0	0	1	1	1	1	0

Synopsis

TDZ clears all internal variables of one Tone detector cell including filter local variables and energy estimator. This command must be sent after changing coefficients of a cell to avoid instability.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	0..3	0..F	Tone detector cell number

TGEN - Enable/disable tone generators

Opcode : 0D

0	0	0	0	1	1	0	1

Synopsis

TGEN causes the ST75C50 to enable or disable the four tone generators.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_0_ENA	1	0	0* 1	Generator #0 disabled Generator #0 enabled
TONE_1_ENA	1	1	0* 1	Generator #1 disabled Generator #1 enabled
TONE_2_ENA	1	2	0* 1	Generator #2 disabled Generator #2 enabled
TONE_3_ENA	1	3	0* 1	Generator #3 disabled Generator #3 enabled

TONE - Predefined tones

Opcode : 0C

0	0	0	0	1	1	0	0

Synopsis

TONE programs the tone generators for the predefined tones. The tone generators #0 and eventually #1 are reprogrammed with this command. Eventualy the tone generator #0 and #1 are enabled. Using an argument not in the following table will disable tone generator #0 and #1.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_SELECT	1	5..0	0 1 2 3 4 5 6 7 8 9 A B C D E F 10* 11 12 13	DTMF 0 (941 & 1336 Hz) DTMF 1 (697 & 1209 Hz) DTMF 2 (697 & 1336 Hz) DTMF 3 (697 & 1477 Hz) DTMF 4 (770 & 1209 Hz) DTMF 5 (770 & 1336 Hz) DTMF 6 (770 & 1477 Hz) DTMF 7 (852 & 1209 Hz) DTMF 8 (852 & 1336 Hz) DTMF 9 (852 & 1477 Hz) DTMF A (697 & 1633 Hz) DTMF B (770 & 1633 Hz) DTMF C (852 & 1633 Hz) DTMF D (941 & 1633 Hz) DTMF * (941 & 1209 Hz) DTMF # (941 & 1477 Hz) Answer Tone (2100 Hz) Answer Tone (1650 Hz) Answer Tone (2225 Hz) Tone (1300 Hz)

V22L2 - V22 loop 2 generator/detector

Opcode : 24

0	0	1	0	0	1	0	0

Synopsis

V22L2 selects the transmission and detection of V.22/V.22bis patterns required for remote digital loop back as defined in the CCITT specification. The STA_V22L bit in the STA_LOOP optional status word will follow the detection of the receiver setting. This command must only be used in V.22 or V.22bis modes.

Note that the STA_V22A bit (alternate "1010" or "0101") in the STA_LOOP is always active.

Parameters

Field	Byte	Pos.	Value	Definition
V22L2_TX	1	0..1	00* 01 10 11	Data mode Transmit unscrambled "1" Transmit scrambled "1" Transmit scrambled "1010"
V22L2_RX	2	0	0* 1	Detect unscrambled "1" Detect scrambled "1"

V54 - Generator/detector

Opcode : 23

0	0	1	0	0	0	1	1

Synopsis

V.54 selects the transmission and detection of V.54 patterns required for remote digital loop back as defined in the CCITT specification. The STA_V54D bit in the STA_LOOP optional status word will follow the detection of the receiver setting. This command must only be used in V.32 or V.32bis modes.

When the transmit generator completes the required pattern it will continue to send the same sequence and set the STA_V54E bit in the STA_LOOP.

Parameters

Field	Byte	Pos.	Value	Definition
V54_TX	1	0..1	00* 01 10 11	Data mode Transmit 2048 V54 scrambled "0" Transmit 1948 V54 scrambled "1" Transmit 8192 V54 scrambled "1"
V54_RX	2	0..1	00* 01 10 11	No V54 detection Reserved Detect 256 V54 scrambled "0" Detect 256 V54 scrambled "1"

XMIT - Start/stop transmission

Opcode : 01

0	0	0	0	0	0	0	1

Synopsis

XMIT enables or disables the transmission of the data according to the selected mode (serial or parallel).

Parameters

Field	Byte	Pos.	Value	Definition
TX_START	1	0	0 1	Stop transmission Start transmission

WMR - Write MAFE Register

Opcode : 11

0	0	0	1	0	0	0	1

Synopsis

WMR allows the writing of a 8-bit parameter into one of the ST7543 MAFE chip register.

Parameters

Field	Byte	Pos.	Value	Definition
MWR_DATA	1	0..7		Byte od data
MWR_ADDR	2	0..1		Byte of the 2-bit address
MWR_RXTX	3	0..7	0 <> 0	Acess Tx Register Access Rx Register

This command must be used to lock the Transmit clock on an external clock or the received clock :

WMR D8 02 00 Tx Clock locked on TxSCLK input Pin.
WMR F8 02 00 Tx Clock locked on Rx Clock.
WMR C0 02 00 Tx Clock free running

APPENDIX B : STATUS DESCRIPTION

This appendix is dedicated to the ST75C50 reporting features. In the following sections are explained the command acknowledge process and the report and status definitions.

I - COMMAND ACKNOWLEDGE AND REPORT

I.1 - Command Acknowledge Process

The ST75C50 features an acknowledge process based on a counter COMACK. On power-on reset, this counter's value is set to 0. Each time a command is executed, the acknowledge counter COMACK is incremented. This allows a precise monitoring of the command entered and avoids command collision.

The acknowledge counter is incremented as soon as the command has been properly executed. Furthermore, the ST75C50 resets the value of the COMSYS register. The interruption IT6 is raised just after the counter is incremented.

In the case of a memory reading command (CR, MR or PPR), the process is slightly different. The command entered is executed, the report area is then filled and the acknowledge counter is incremented afterwards. This insures that the controller reads the value corresponding to its request. Figure B1 gives a flowchart of the command acknowledge process.

I.2 - Reports Specification

The report section of the Dual Port RAM is dedicated to memory reading. In response to a CR, MR, IDT or PPR command, the value to be read is transferred to the Report registers COMREP[0..1].

I.2.1 - CR COMMAND

Issuing a CR command causes the ST75C50 to dump a specific memory location in complex mode. This instruction is particularly useful for equalizer state analysis or for software eye-pattern display. The report area has this meaning :

RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0	COMREP[0]

IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	COMREP[1]

RP7..RP0 is the MSB part of the 16-bit value of the real part and IP7..IP0 is the MSB part of the imaginary part. The CR command insures that the real and imaginary parts of the desired complex value are sampled internally at the same time. The address given in the parameter field of CR is the address of the real part.

I.2.2 - MR/TDRC/IDT COMMAND/IDT

The report issued by the MR/TDRC command is followings the same rules as the CR. The report meaning is :

D7	D6	D5	D4	D3	D2	D1	D0	COMREP[0]

D15	D14	D13	D12	D11	D10	D9	D8	OMREP[1]

D15..D0 is the 16-bit value required by the MR/TDRC command.

I.2.3 - PPR COMMAND

The PPR command issues the following report :

0	0	0	0	PP3	PP2	PP1	PP0	COMREP[0]

PP0..PP3 are the values read on the 4 pins of the parallel port. The result doesn't take into acccount the fact that those pins are input or output pins.

II - ERROR STATUS

The error status is changed each time an error occurs or an important change in the data pump state occurs. Several events are flagged by the SYSERR byte. They can only be cleared by the CSE command.
The meaning of the SYSERR byte is :

SYSERR		
Field	**Pos.**	**Meaning when set**
ERR_TX	0	Tx buffer underflow or improper buffer status
ERR_RX	1	RX buffer overflow or improper buffer status
ERR_SYM	2	Symbol buffer synchronization error
ERR_IOCD	3	Incorrect opcode
ERR_IPRM	4	Incorrect parameter for current command
Reserved	5	Reserved for future use
Reserved	6	Reserved for future use
ERR_RTK	7	Real time kernel error

III - GENERAL STATUS

The general status is made of two bytes. The first is dedicated to the CCITT circuit monitoring, as well as some line-side information. The second byte is dedicated to the pump state.

Each status word, when changing, can generate an IT4 interrupt. Using the **DSIT** command allows the user to selectively mask the relevant bits. The default values for the mask are 0X3F for STATUS [0] and 0XFF for STATUS [1].

STATUS[0]		
Field	**Pos.**	**Meaning when set**
STA_109	0	CCITT circuit 109 on / DCD : when set indicates that valid data are received, when reset the data are clamped to constant mark.
STA_107	1	CCITT circuit 107 on / DSR
STA_106	2	CCITT circuit 106 on / CTS : when set indicates that the training sequence has been completed and that any data at TxD (serial Mode) or in the Tx Buffer (paralle Mode) will be transmitted.
STA_RING	3	Ring detected : when set a ring signal (from 15Hz to 68Hz) is present at the RING Pin. Note that the precise frequency can be read in the DSP RAM.
STA_CPT0	4	Call progress tone detector #0 triggered (Low Pass)
STA_CPT1	5	Call progress tone detector #1 triggered (Hi Pass)
STA_CPT10	6	Band 0 higher in level then band 1 (Low > Hi)
STA_109F	7	Fast Carrier Detect : this signal reflect the carrier energy received on the line according with the carrier detect threshold and hysteresis

STATUS[1]			
Field	**Pos.**	**Value**	**Meaning**
STA_H	1..0	00 01 10	Not in handshake mode Handshake in progress Handshake timeout
STA_AT	3..2	00 10 11	No answer tone detected Bell answer tone detected CCITT answer tone detected/or AA detected
STA_RTRN	4	0 1	No remote retrain detected V.32/V.22b Remote retrain detected
STA_SYNC	4	1	FAX : synchronization in Progress
STA_RNEG	5	0 1	No remote rate negotiation detected (V.32b) Remote rate negotiation detected
STA_CLR	6	0 1	No cleardown detected Cleardown detected
STA_DTMF	7	0 1	DTMF digit not detected (DTMF Rx mode) DTMF digit detected

IV - QUALITY STATUS

The STAQUA byte monitors an evaluation of the line quality. It is updated once per baud and its value ranges from 127 (perfect quality) to 0 (terrible quality). This provides valuable information about the safety of the transmission (error sensitivity). The Quality Indicator is LSB adjusted.

STAQUA			
Field	**Pos.**	**Value**	**Meaning**
STA_Q	6..0	0..127	Quality index
Reserved	7		Reserved for future use

V - OPTIONAL STATUS

The ST75C50 allows the host to monitor 3 memory locations inside the memory spaces of the DSP. Those locations are updated once per baud. On Power-on Reset, default locations are preprogrammed for the STAOPT[0..2] bytes. The meaning of this default setting is :

STAOPT[0..2]			
Field	**Byte**	**Pos.**	**Meaning**
NEG_MODE	0	7..0	Negotiated speed mode (see below)
LOOP_STA	1	7..0	Test loops status (see below)
HDSK_PHA	2	7..0	Handshake phase (range 0..255)

After configurating the ST75C50 in a Modem mode, by sending a CONF command the default STAOPT are preprogrammed to :

Default STAOPT[0..2] after a CONF Modem Command			
Field	**Byte**	**Pos.**	**Meaning**
NEG_MODE	0	0..7	Negotiated speed mode (see below)
LOOP_STA	1	0..7	Test loops status (see below)
HDSK_PHA	2	0..7	Handshake phase (range 0..255)

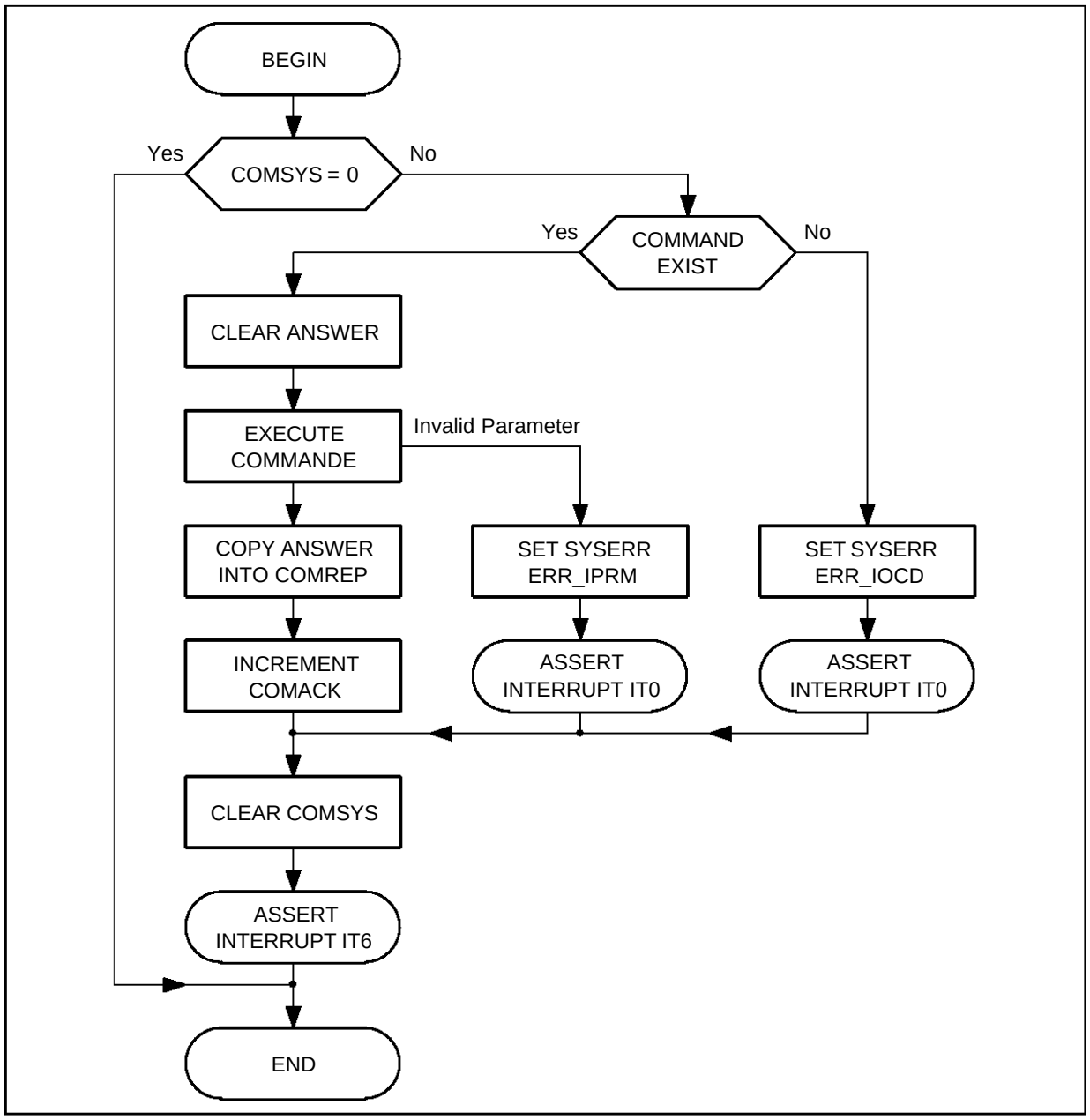
The NEG_MODE byte indicates the issue of the rate negotiation. Its meaning is :

NEG_MODE			
Field	**Pos.**	**Value**	**Definition**
NEG_PRG	0	0 1	Negotiation in progress Negotiation completed
NEG_SPEED	4..1	0 1 2 3 4 5 6 7 8 F	Negotiated speed is 300bps Reserved Negotiated speed is 1200bps Negotiated speed is 2400bps Negotiated speed is 4800bps Negotiated speed is 7200bps Negotiated speed is 9600bps Negotiated speed is 12000bps Negotiated speed is 14400bps Negotiation failed
NEG_TREL	5	0 1	Negotiated mode is not trellis coded Negotiated mode is trellis coded
NEG_MODU	6	1 0	Negotiated mode is FSK Negotiated mode is QAM/DPSK
NEG_STD	7	0 1	CCITT Std. Bell Std. (103 or 212A)

The loop status byte provides valuable information about the loop status, for V.22 and V.54 loops. This status byte must be used in accordance with the V22L2 or V54 commands. Its meaning is :

STA_LOOP		
Field	**Pos.**	**Meaning when set**
STA_V54D	0	V.54 pattern detected : when set, a 256 bit V.54 pattern has been received.
STA_V54E	1	V.54 pattern completed : when set, the transmit V.54 pattern is completed.
STA_V22A	2	V.22bis alternate ”0101” or ”1010” detected (typically 53ms)
STA_V22L	3	V.22bis loop pattern detected (typically 13ms)
Reserved	7..4	Reserved for future use

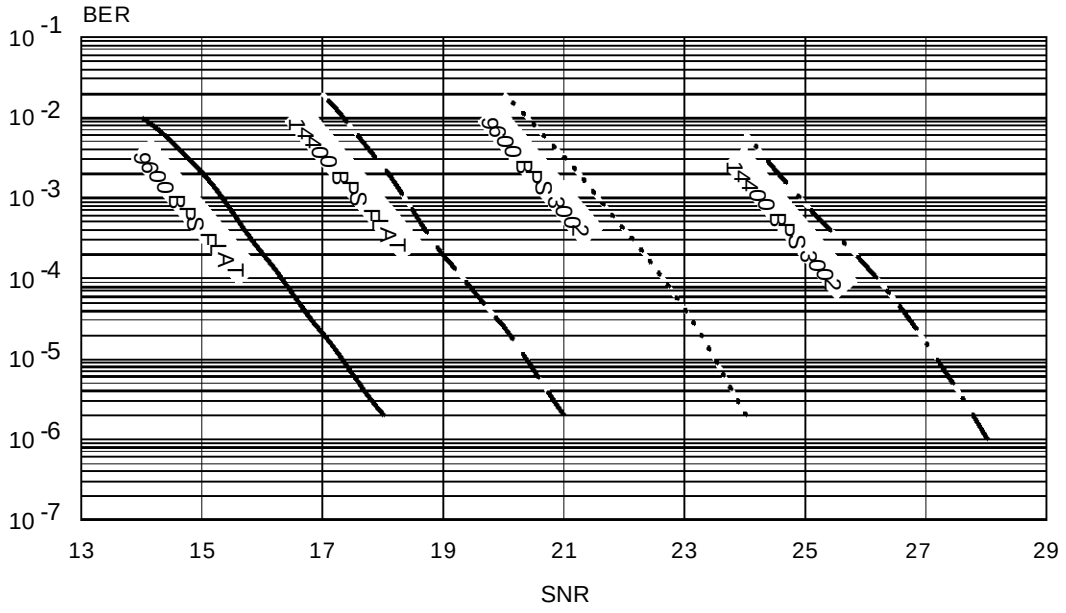
Figure B1


BEGIN
Yes
COMSYS = 0
No
Yes
COMMAND EXIST
No
CLEAR ANSWER
EXECUTE COMMANDE
Invalid Parameter
COPY ANSWER INTO COMREP
SET SYSERR ERR_IPRM
SET SYSERR ERR_IOCD
INCREMENT COMACK
ASSERT INTERRUPT IT0
ASSERT INTERRUPT IT0
CLEAR COMSYS
ASSERT INTERRUPT IT6
END
75C50-07.EPS

APPENDIX C : TYPICAL BER PERFORMANCES

This appendix shows the typical Bit Error Rate curves obtained on lines Flat and US3002, using a TAS® Series II equipment and a V.56 AGC. Sample size is 10^7 bit.

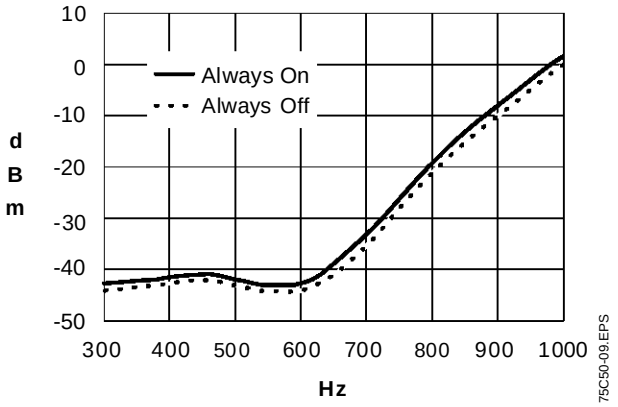
Figure C1 : Typical V32bis BER performances



75C50-08.EPS

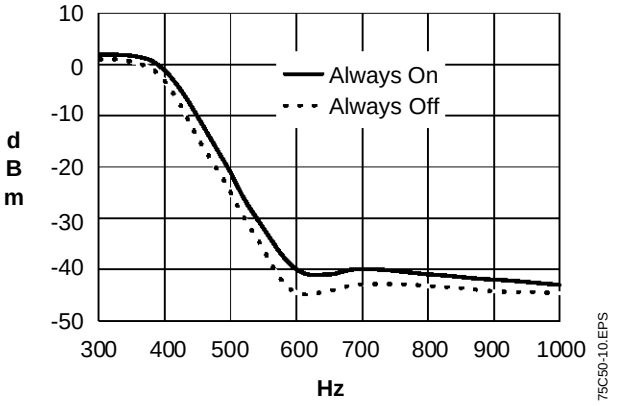
APPENDIX D : DEFAULT CALL PROGRESS TONE DETECTORS

Figure D1 : Call Progress Tone Detector Band 0



75C50-09.EPS

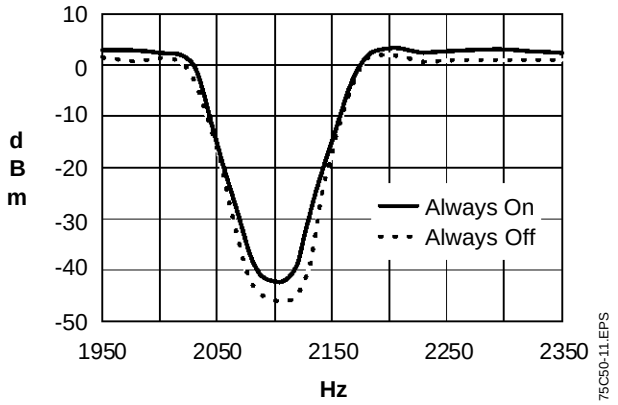
Figure D2 : Call Progress Tone Detector Band 1



75C50-10.EPS

APPENDIX E : DEFAULT ANSWER TONE DETECTORS

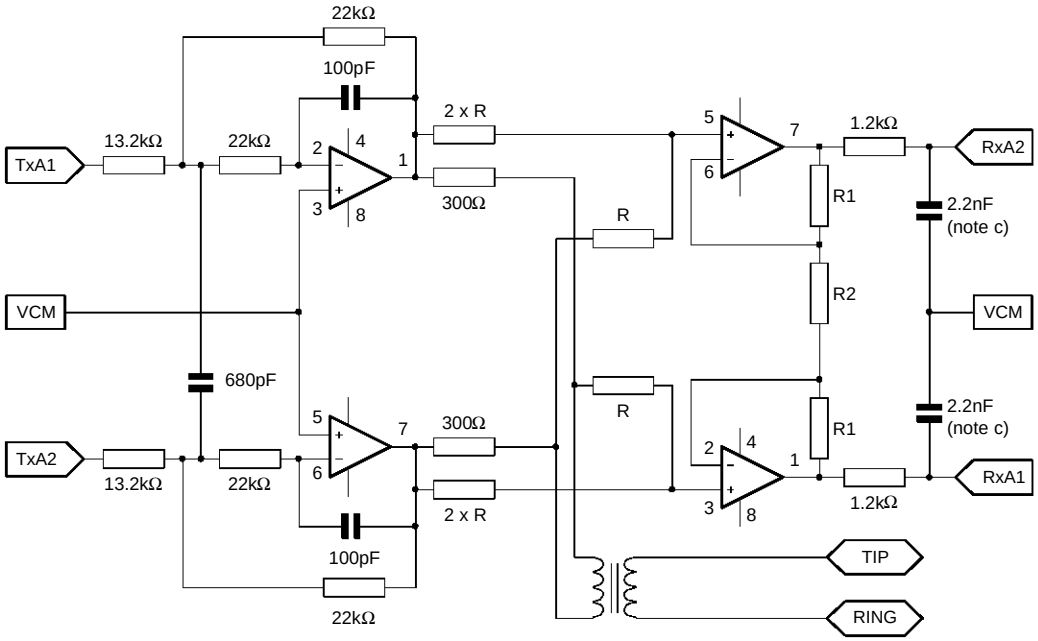
Figure E1 : 2100Hz Answer Tone Detector



APPENDIX F : ELECTRICAL SCHEMATICS

This appendix contains the following schematics :
- example of hybrid line design
- chip interconnect circuitry required in the case of the minimal configuration
- interconnect circuitry required for the use of the serial link (TS7538) as well as a bulk delay memory.
- emulation using external program memory

Figure F1 : Typical line interface



Notes : a) All resistors are 1% tolerance
b) The receive gain is defined by : G = (1 + R1/R2)
c) Capacitor close to RxA1 and RxA2

Figure F2

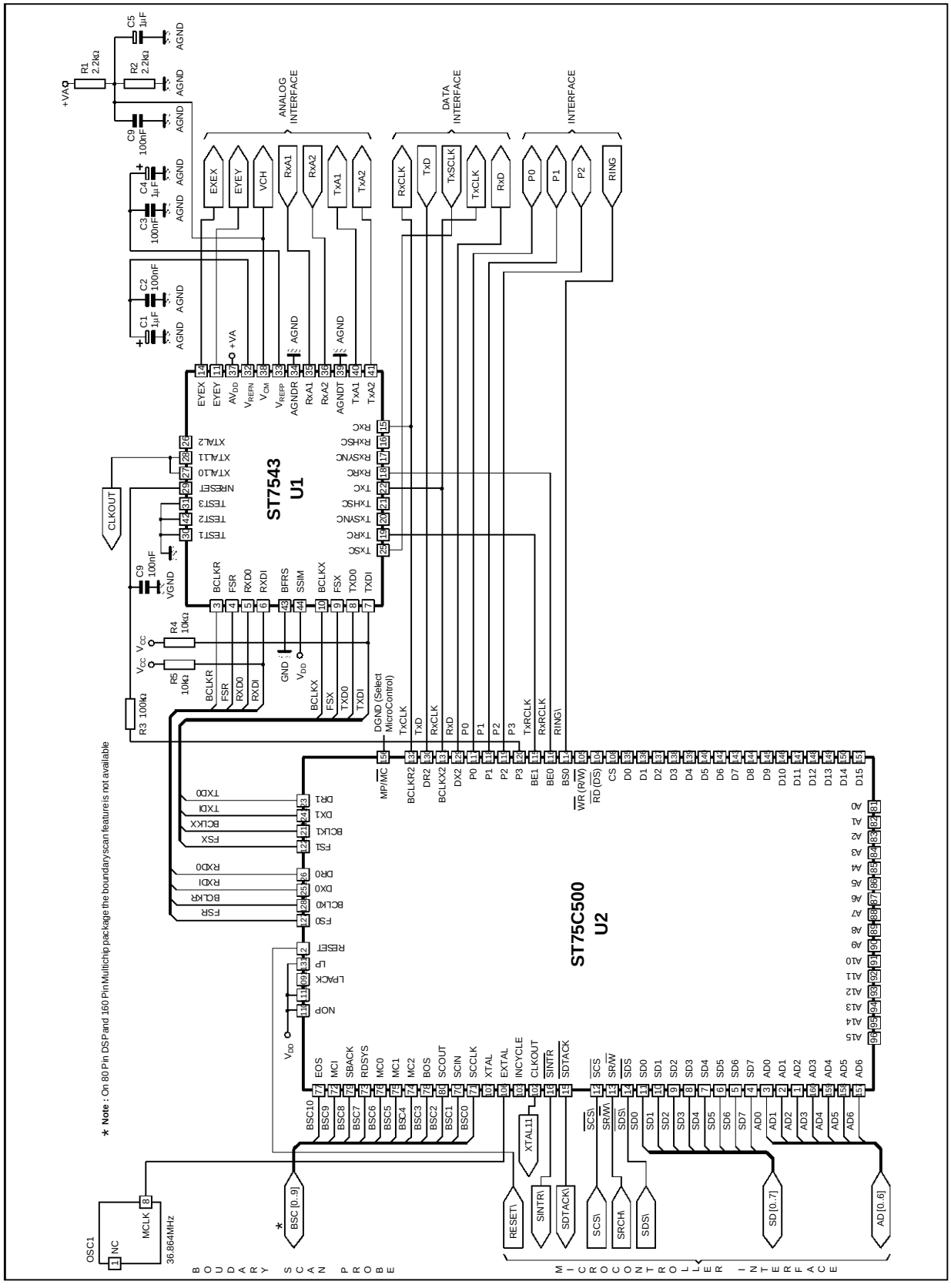

ST7543
U1
ST75C500
U2
ANALOG INTERFACE
DATA INTERFACE
INTERFACE
CLKOUT
DGND (Select MicroControl)
* Note : On 80 Pin DSP and 160 Pin Multichip package the boundary scan feature is not available
BOUNDARY SCAN PROBE
MICROCONTROLLER INTERFACE
36.864MHz
75C50-13.EPS

Figure F3

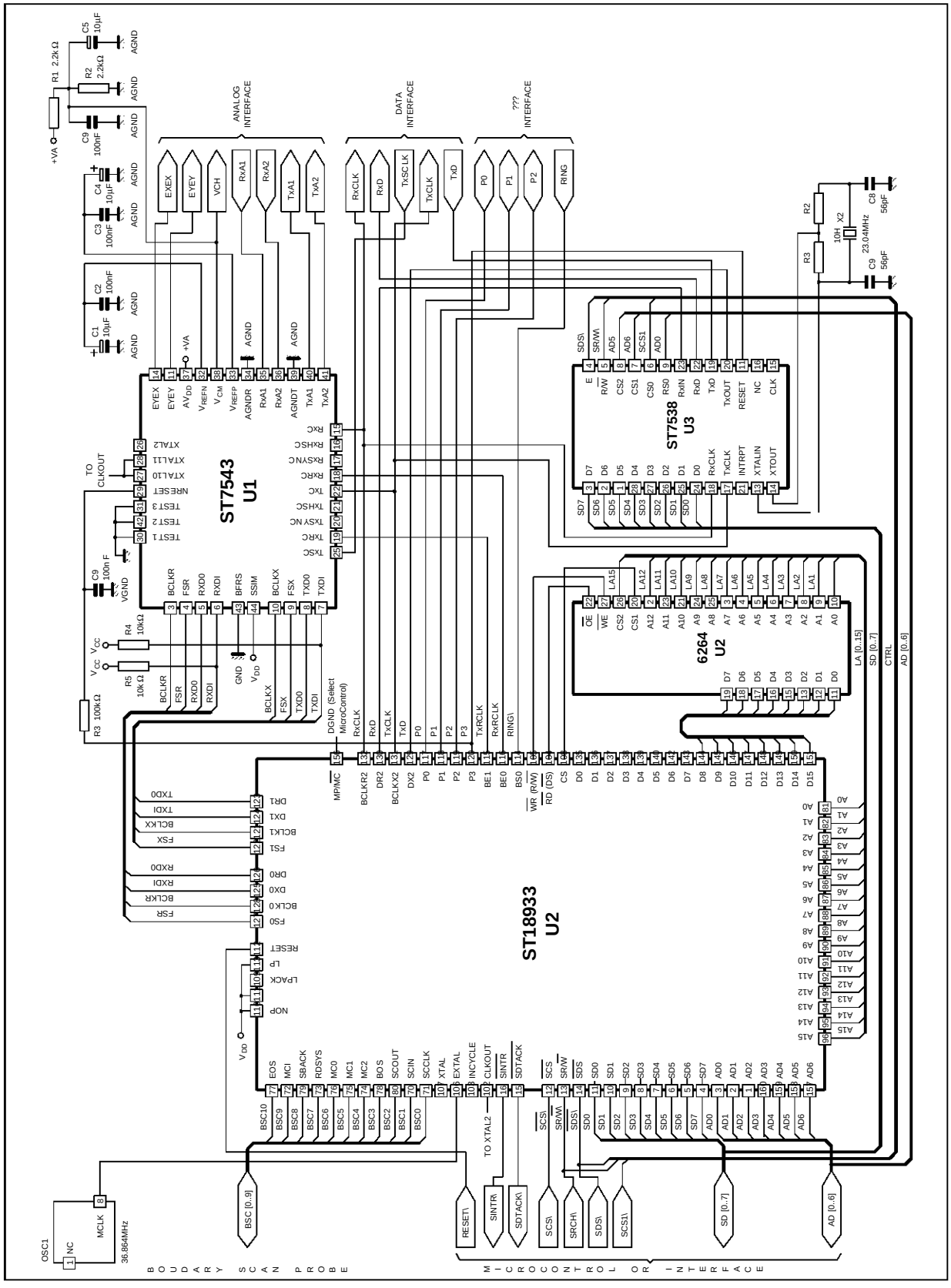
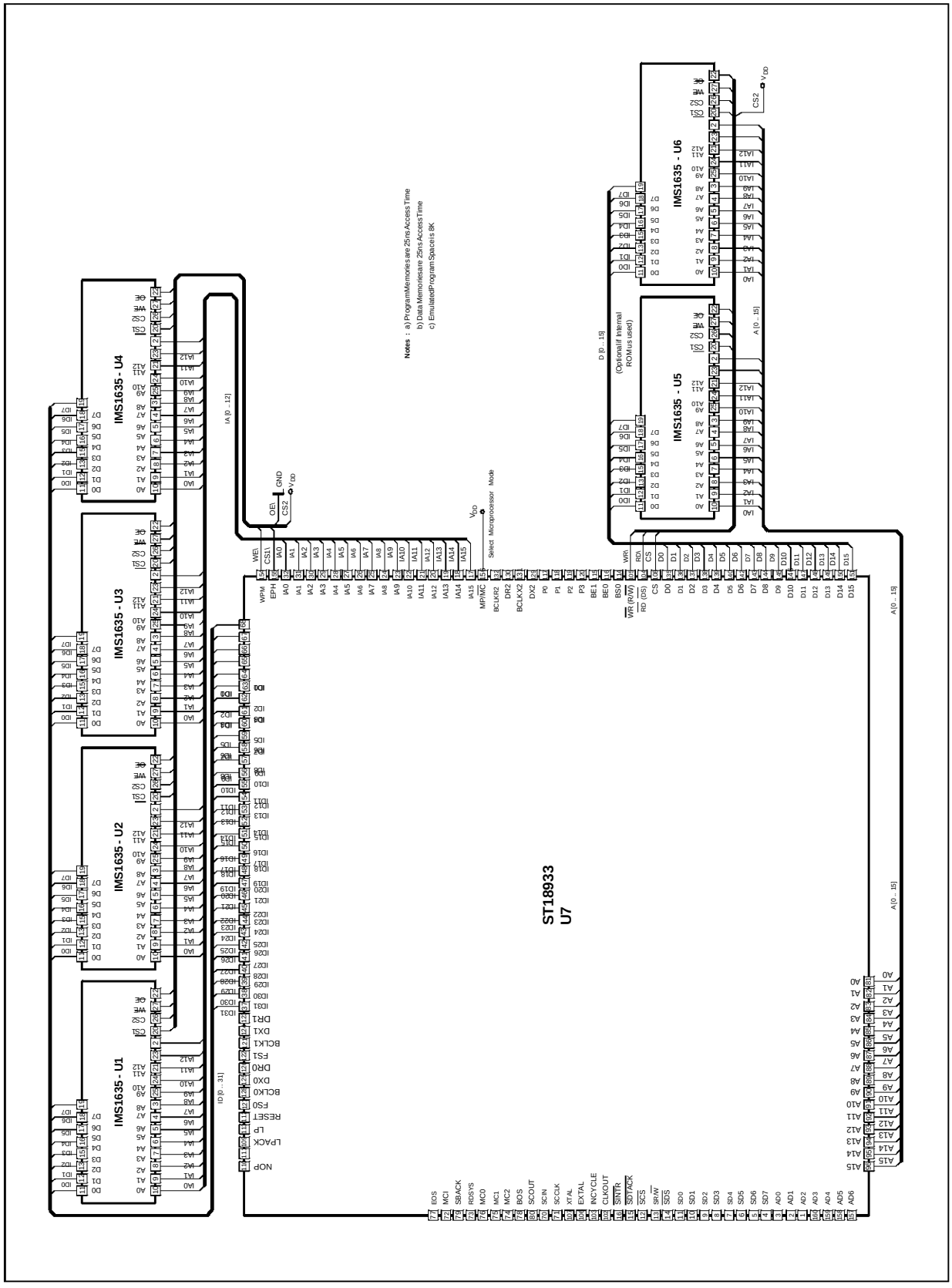

ST7543
U1
ST7538
U3
6264
U2
ST18933
U2
ANALOG INTERFACE
DATA INTERFACE
??? INTERFACE
BOUNDARY SCAN PROBE
MICROCONTROLLER INTERFACE
75C50-14.EPS

Figure F4



75C50-15.EPS

APPENDIX G

I - TONE DETECTORS

I.1 - Overview

The general purpose TS75C50/51/52 tone detector block is a powerful module that covers a lot of applications :

- Call progress tone detection, fully programmable for all different countries
- DTMF detection
- High level handshake for all main modem standards
- FAX, voice, data automatic detection
- Call waiting detection, while in voice or data mode

I.2 - Description

The tone detector block is a set of 16 identical cells. Each cell is composed of a double biquadratic filter, a power estimator section, a static level and a level comparator.

Each biquadratic filter, power estimator and static level can be programmed using a complete set of commands (TDRC, TDRW, TDWC, TDWW, TDZ).

The wiring between the different cells can be defined by the user using the command allowing a wide range of applications.

The 16 comparator outputs give, on a baud basis, the information into a two 8 bits word TONEDET0 (for cells number 0 to 7) and TONEDET1 (for cells number 8 to F). These TONEDET variables can be accessed using a MR command or, more easily, monitored on a baud basis using the DOSR command.

While in FAX half duplex receive IDLE mode a set of 8 cells allows to implement customized handshake short sequences.

I.2.1 - BIQUADRATIC FILTERS (see Figure G1)

Each biquadratic filter is a double regular section that can perform any transfer function with 4 poles and 4 zeros. This routine is run on a sample basis.

The corresponding transfer function is :

$$\frac{Out}{Input} = C0 \cdot \frac{C5 + 2 \cdot C3 \cdot z^{-1} + 2 \cdot C4 \cdot z^{-2}}{1 - 2 \cdot C1 \cdot z^{-1} - 2 \cdot C2 \cdot z^{-2}} \cdot C6 \cdot \frac{CB + 2 \cdot C9 \cdot z^{-1} + 2 \cdot CA \cdot z^{-2}}{1 - 2 \cdot C7 \cdot z^{-1} - 2 \cdot C8 \cdot z^{-2}} \cdot z^{-1}$$

Note : All coefficients are coded on 16 bits 2's complement in the range +1, -1 (Q15). To avoid the possibility of overflow the user must check that the internal node must not be higher that 0.5 (in Q15 representation).

I.2.2 - POWER ESTIMATION (see Figure G2)

The power estimation cell is needed to measure the amplitude of the different tones. It is run on a sample basis.

The corresponding transfer function is :

$$Out = |Input| \cdot z^{-1} \cdot \frac{P1}{1 - (1 - P1) \cdot z^{-1}}$$

Note : To deal with the high dynamic range of the analog front end, the computation loop of the power estimation is run with 32 bits accuracy. The output and input of that cell are however 16 bit words (Q15).

Figure G1 : Biquadratic IIR Filter

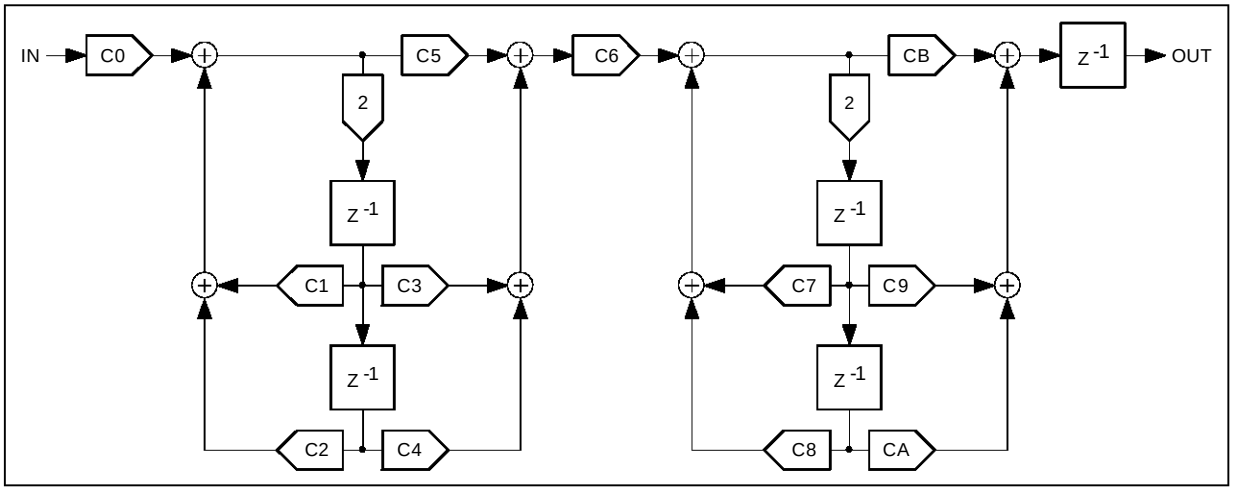
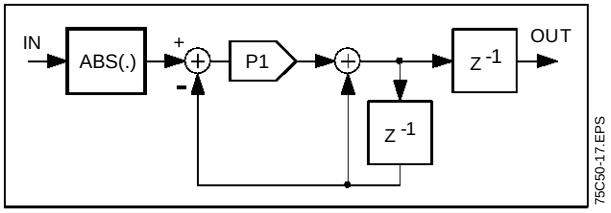


Figure G2 : Power Estimator



I.2.3 - STATIC LEVEL

A single threshold level is associated with each cell. It can be use to compare the output of a power estimation with an absolute value.

I.2.4 - COMPARATOR

The comparator computes on a baud basis, the difference of the signal on its positive input and its negative input. If the result is higher that zero it set the corresponding bit in the TONEDET[0..1] word if not it clears this bit.

I.2.5 - WIRING

The user must specify the connection (wiring) between the input/output of the filter, the input/output of the power estimator, the output of the static levels and the two inputs of the comparators.

The outputs signal have an absolute address :

Node Address		
Signal Name	**Address**	**Description**
Ground	00	Signal always equal to 0000
RxSig	01	Receive signal from the analog front end, (after echo-substraction in V.32 mode)
RxSig2	02	Receive signal multiplied by 2
RxSig4	03	Receive signal multiplied by 4
	04..0F	Reserved
Filter [0..F]	10..1F	Biquadratic filter outputs
Power [0..F]	20..2F	Power estimator outputs
Level [0..F]	30..3F	Static levels

The user specifies the inputs of the filters, power and comparators. At least one input must come from the RxSig (node 01, 02 or 03). It is mandatory to connect all unused cell input to the ground signal (node 00).

III - EXAMPLE (see Figure G5)

Hereunder is an example of programming a single tone detector (using cell #3) and a complex differential tone detector (using cell #4 and #5).

The bit 3 of the TONEDET variable will be triggered each time the energy of that filtered signal is higher than static level number 3.

The bit 4 of the TONEDET variable will be on each time a receive signal has energy higher than the static level number 4. The bit 5 will be on only when the filtered (filter section 4 and 5) received signal is higher than the energy of the wideband signal number 4 ; this prevents triggering on noise.

Program cell #3 :

TDWW 03 00 13 01
Connect received signal to filter and filter to energy
TDWW 03 01 33 23
Connect level to comparator negative input and energy to positive input

Program cell #4 and #5 :

TDWW 04 00 01 01
Connect received signal to filter and energy
TDWW 04 01 34 24
Connect level to comparator negative input and energy to positive input
TDWW 05 00 15 14
Connect filter #4 output to filter and filter to energy
TDWW 05 01 24 25
Connect wideband energy to negative input and energy to positive input

Figure G3 : Tone Detector Wiring Address (first half)

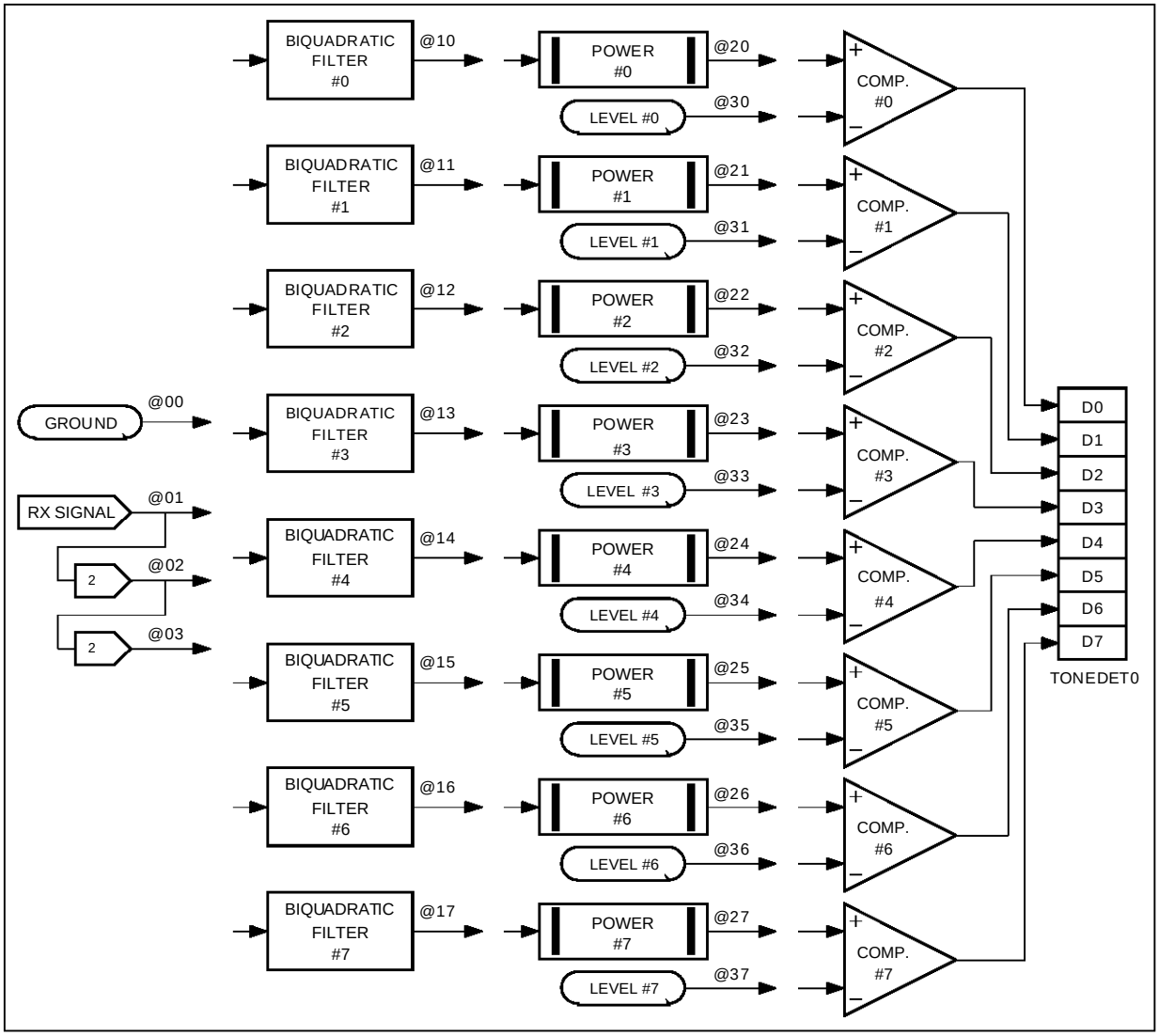


Figure G4 : Tone Detector Wiring Address (second half)

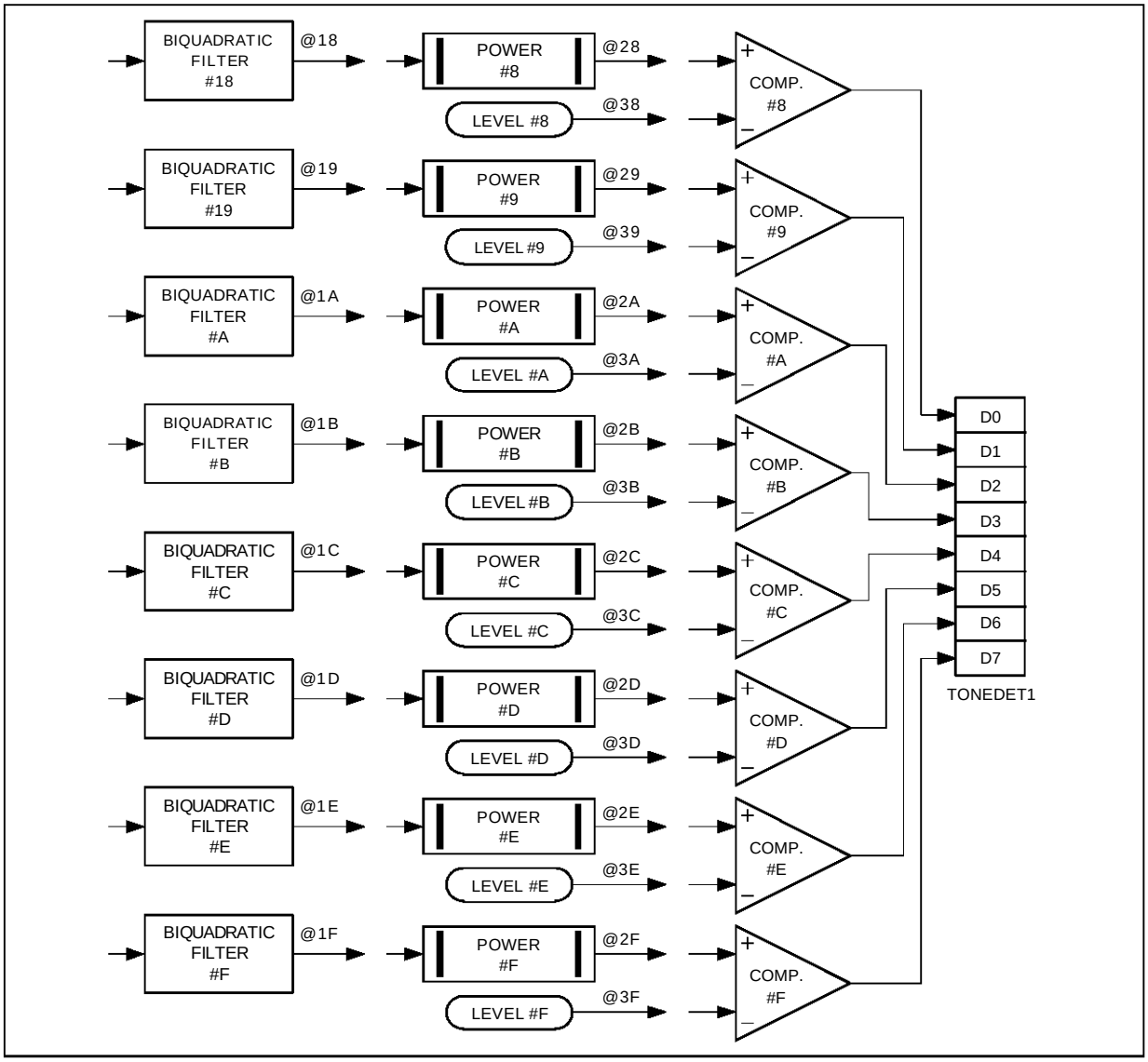
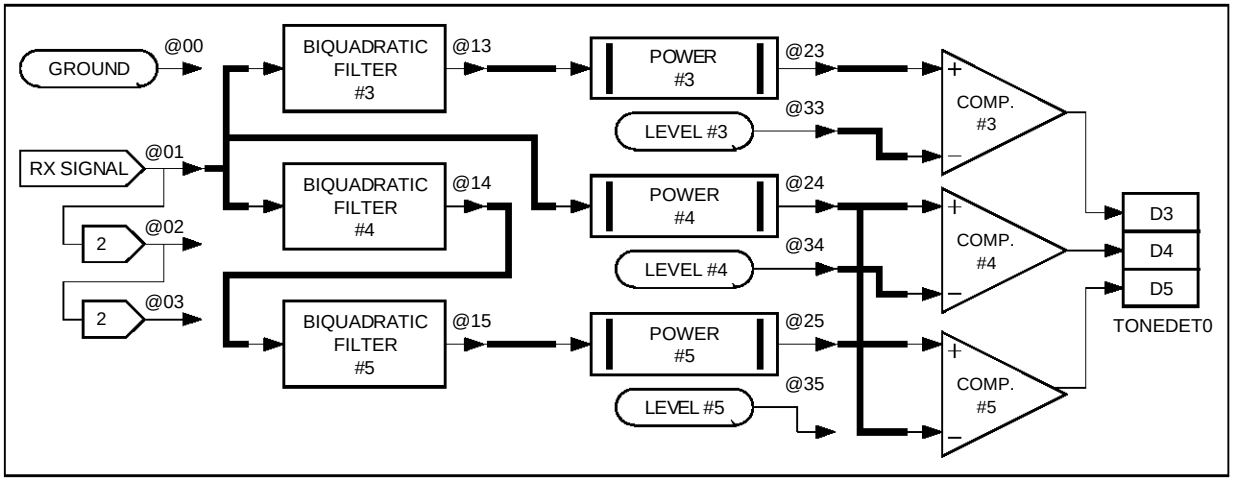


Figure G5 : Wiring Example



APPENDIX H : BUFFER OPERATIONS

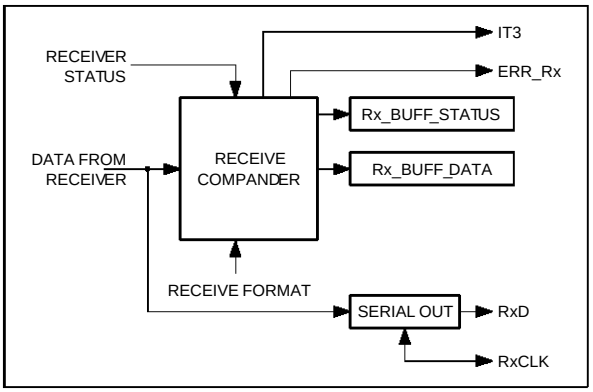
I - INTRODUCTION

This appendix is dedicated to the buffer operations, either the data buffers, used either in data exchanges or the symbol buffer operations dedicated to bulk delay management.
The first part is oriented towards a functional description of the buffer operations, while the second section is more oriented towards the management of the buffers.

II - RECEIVE OPERATIONS OVERVIEW

Figure H1 describes the receive data flow.

Figure H1 : Rx Buffer Schematics



The ST75C50 uses parallel synchronous data.
8 bit words are synchronously available in the receive buffers. The buffer status holds the numbers of valid bytes received.

Each time the receive compander has filled up a new buffer, it sets the corresponding flag with the proper status then generates the IT3 interrupt. The availability of the buffers is tested just before starting to fill them. This means that the host must not perform any buffer operation on the data part while the status remains 0.

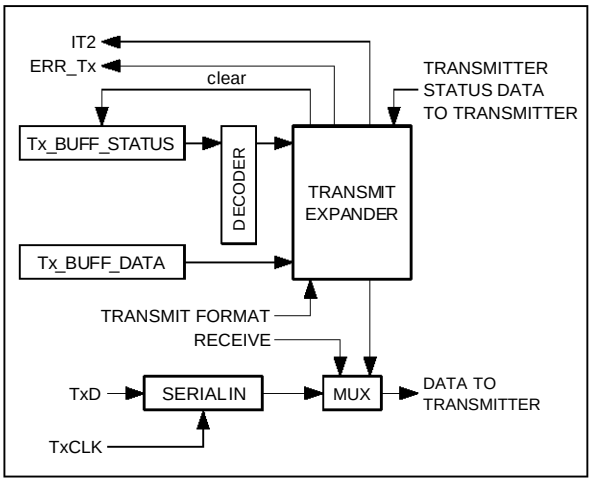
III - TRANSMIT OPERATIONS OVERVIEW

Figure H2 describes the transmit data flow.

The ST75C50 uses parallel synchronous data.
8 bit words are synchronously read from the transmit buffers. The transmit status buffer holds the number of valid bytes to be transmitted (up to 8 per buffer).

Each time the transmit expander has emptied a buffer, the IT2 interrupt is raised.

Figure H2 : Tx Buffer Schematics



IV - BUFFER STATUS AND FORMAT DESCRIPTION

The following section describes the meaning and use of the buffer status words.

IV.1 - Transmit buffer

The transmit buffer status words are DTTBS0 and DTTBS1 (see the *Host Interface Summary* section in the main document) and are more likely to be seen as control words. These flags must be set by the host and are reset by the ST75C50. The data buffer exchanges being synchronized through these status words, an improper setting will trigger the error Err_Tx in the error status SYSERR. A value of 0 for DTTBS0 or DTTBS1 means that the corresponding buffers are empty : this value is written by the ST75C50. The unused bits of DTTBSx must be set to 0 by the host.

Field	Pos.	Val.	Description
BUFF_LENG	3..0	8..1	Number of valid bytes in the buffer

IV.2 - Receive buffer

The receive buffer status words are DTRBS0 and DTRBS1 (see the *Host Interface Summary* section in the main document). These flags are set by the ST75C50 and must be reset by the host. The data buffer exchanges being synchronized through these status words, an improper resetting will trigger the error Err_Rx in the error status SYSERR. A value of 0 for DTRBS0 or DTRBS1 means that the corresponding buffers are empty : this value must be written by the host.

Field	Pos.	Val.	Description
BUFF_LENG	3..0	8..1	Number of valid bytes in the buffer

V - DATA BUFFER MANAGEMENT

In the transmit path, the data buffer exchanges should always begin with the filling of buffer 0, then with the update of the buffer 0 status word. The initiation of the data exchanges is initiated then with the XMIT command.

VI - BULK DELAY MANAGEMENT

The processing of the bulk delay uses a simplified buffer exchange scheme. Each time the ST75C50 has internally buffered enough symbols, it writes them inside the symbol buffer area, then computes the address inside the host space where these symbols should be written. This address is a relative address inside the host data space, allowing thus the host to dispose this area the most convenient way. The target address is located in the SYMADR[0..1] registers under a 16-bit form.

These addresses must be defined by the user using the BULK command. It can be any valid 16 bit number assuming the base address (BA_ADDR) is on a 8 byte boudary and the top address (TO_ADDR) is higher and on a 8 byte boundary minus 1.

Eg : if we want to be able to cancel a 2 satellites Round trip delay we must have a bulk delay bigger than 2 times 560ms, lets say 1.5 seconds. The symbols needed are 1.5 · 2400 (3600 bytes). If we say that the base address is, for example, 0x4230 the top address must be 0x503F (= 0x4230 + 3600 - 1).

According to the current round trip delay, the ST75C50 computes the address of the symbols required for the far end echo computation. This address is computed (as the previous one) according to a circular addressing scheme inside the base .. top address space.

The symbol buffer status SYSSTA is then set to FF and the IT1 interrupt is raised. The host should then perform the following operations in sequence :

1) read the address SYMADR[0..1] of the target location for the symbols,
2) read SYMBU[0..7], the corresponding symbols, and store them at the addressed lolcation (8 symbols),
3) read the address SYMADT[0..1] of the symbols required by the ST75C50,
4) fetch the required 8 symbols and store them in the SYMBUF[0..7] array,
5) write the proper status word (00) in SYMSTA.

The ST75C50 meanwhile pools for the status word to be 00, then stores the symbols inside its own memory space for processing and sets the status word to its idle value FF.

VI.1 - Status Word

The status word SYSSTA can have the following values :

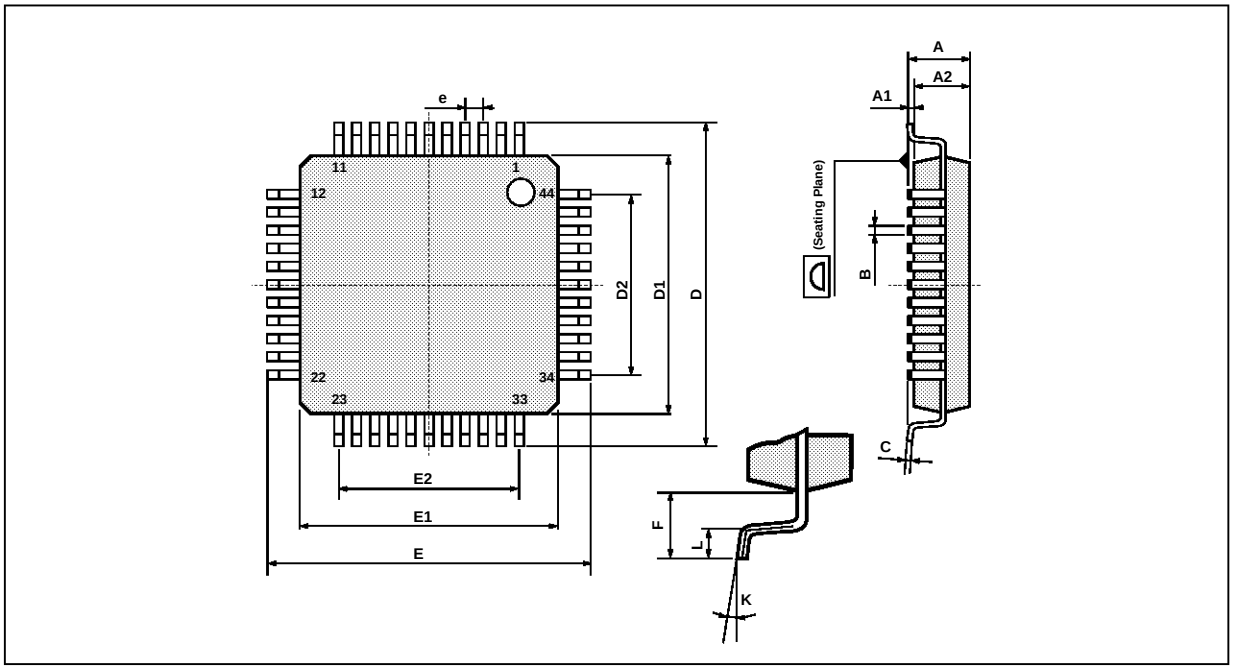
Field	Pos.	Val.	Description
SYSTA	7..0	00	Symbol buffer owned by the DSP
		FF	Symbol buffer owned by the host

VI.2 - Interrupt

Each time a symbol buffer is processed by the ST75C50 an IT1 interrupt is generated. The host has an 8 symbols time (3.3ms) to process this interrupt otherwise an error occurs that will be signaled into the SYSERR bit 2 ERR_SYM.

PACKAGE MECHANICAL DATA

44 PINS - PLASTIC QUAD FLAT PACK (THIN)

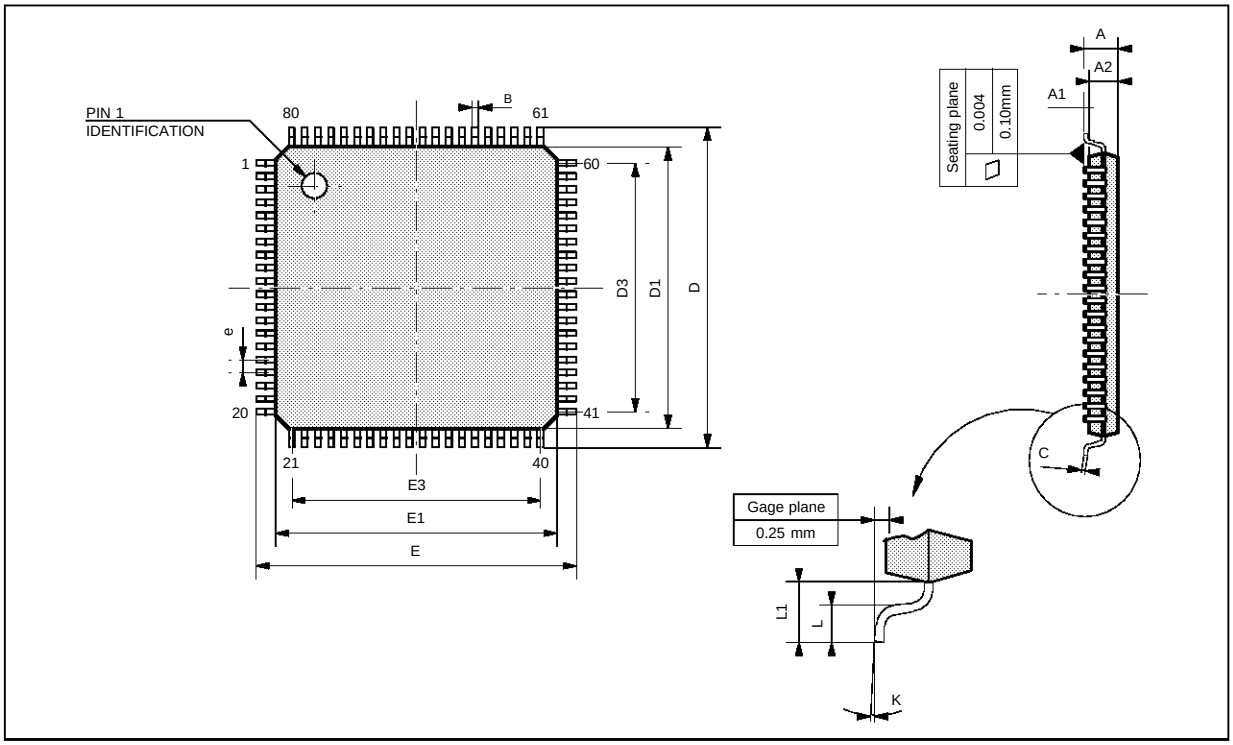


PMPQFP44.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1		0.25			0.01	
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.35		0.50	0.014		0.020
C			0.17			0.007
D	15.75	16.00	16.25	0.620	0.630	0.640
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		10.00			0.394	
e		1.00			0.039	
E	15.75	16.00	16.25	0.620	0.630	0.640
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		10.00			0.394	
F		1.60			0.063	
K	0^o (min.), 7^o (max.)					
L	0.45	0.60	0.75	0.018	0.024	0.030

TQFP44.TBL

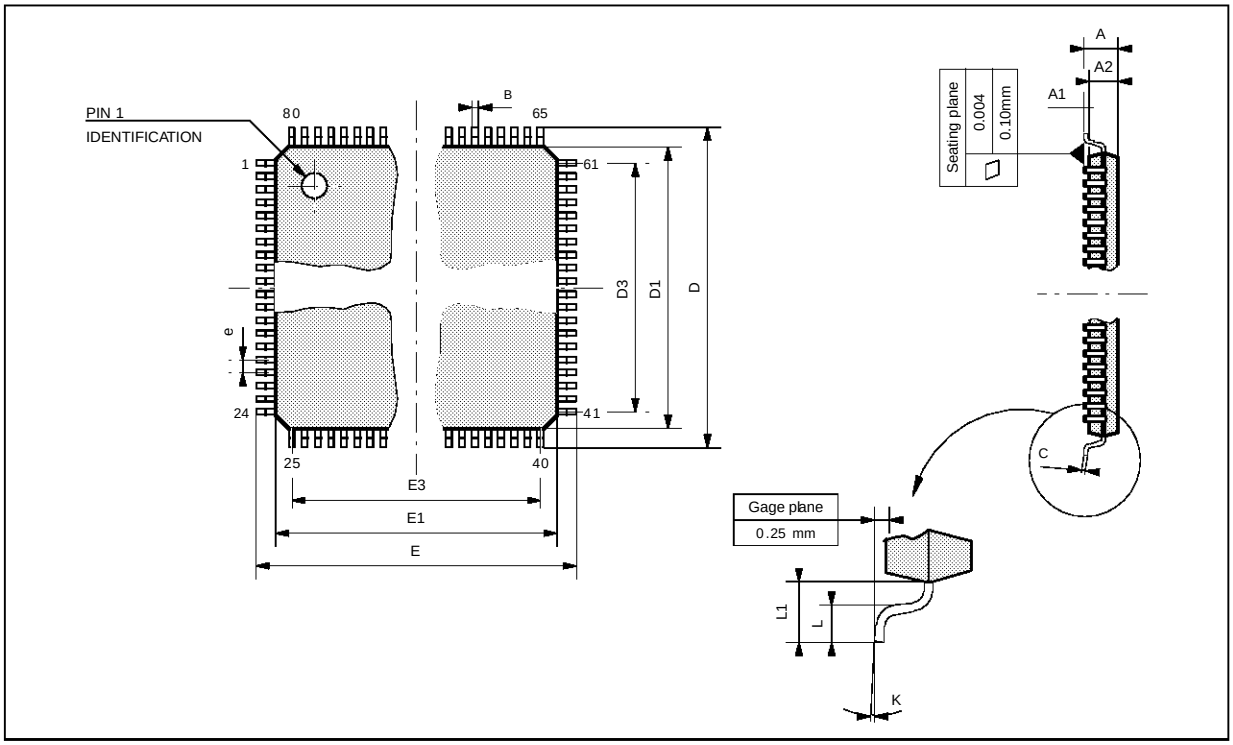
PACKAGE MECHANICAL DATA (continued)
80 PINS - PLASTIC QUAD FLAT PACK (THIN)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.22	0.32	0.38	0.010	0.012	0.014
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.35			0.486	
e		0.80			0.0314	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.35			0.486	
L	0.45	0.60	0.75	0.020	0.024	0.030
L1		1.00			0.039	
K	0^o (min.), 7^o (max.)					

TQFP80.TBL

PACKAGE MECHANICAL DATA (continued)
80 PINS - PLASTIC QUAD FLAT PACK

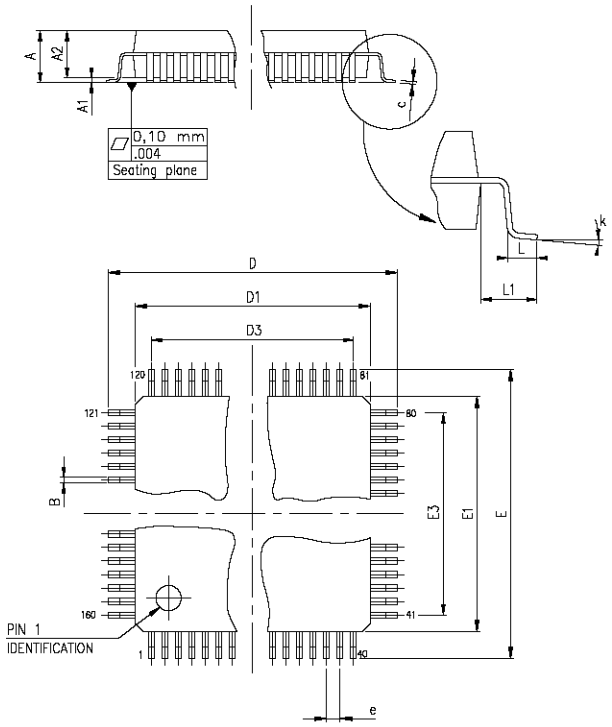


PMPQFP80.EPS

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.30		0.45	0.011		0.018
C	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.903	0.913	0.923
D1	19.90	20.00	20.10	0.785	0.787	0.789
D3		18.40			0.724	
e		0.80			0.0314	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0^o (min.), 7^o (max.)					

PQFP80.TBL

PACKAGE MECHANICAL DATA (continued)
160 PINS - PLASTIC QUAD FLAT PACK



PMPQF160.EPS

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.135	0.145
B	0.22		0.38	0.008		0.015
D	30.95	31.20	31.45	1.218	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		25.35			0.998	
e		0.65			0.0256	
E	30.95	31.20	31.45	1.218	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
E3		25.35			0.998	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0^o (min.), 7^o (max.)					

PQFP160.TBL